TM 11-6625-1833-30

TECHNICAL MANUAL

DIRECT SUPPORT MAINTENANCE MANUAL

TEST SET GROUP, INDICATOR, RADAR OQ-63A/APS-94D (NSN 6625-01-058-7874)

HEADQUARTERS, DEPARTMENT OF THE ARMY

APRIL 1979

WARNING

EXTREMELY DANGEROUS VOLTAGES EXIST IN THIS EQUIPMENT

Be careful when working on any connector of Test Set Group, Indicator, Radar OQ–63A/APS–94D. Test Set Subassembly MX–8638A/APS–94D and Test Set Subassembly MX–9639A/APS–94D contain connectors with terminals carrying 640 volts dc, 531 volts dc, 115 volts ac, and +100 volts dc.

DON'T TAKE CHANCES!

EXTREMELY DANGEROUS VOLTAGES EXIST IN THE FOLLOWING UNITS:

Test Set Subassembly MX–8638A/APS–94D .... +630 vdc
Test Set Subassembly MX–8639A/APS–94D .... +531 vdc

WARNING

The fumes of TRICHLOROETHANE are toxic. Provide thorough ventilation whenever it is used; avoid prolonged or repeated breathing of vapor. Do not use near an open flame or hot surface; trichloroethane is non-flammable but heat converts the fumes to a highly toxic phosgene gas the inhalation of which could result in serious injury or death. Prolonged or repeated skin contact with trichloroethane can cause skin inflammation. When necessary, use gloves, sleeves and aprons which the solvent cannot penetrate.

TECHNICAL MANUAL
NO. 11-6625-1833-30

HEADQUARTERS
DEPARTMENT OF THE ARMY
WASHINGTON, DC 25 April 1979

DIRECT SUPPORT MAINTENANCE MANUAL

TEST SET GROUP, INDICATOR, RADAR OQ-63A/APS-94D (NSN 6625-01-058-7874)

REPORTING OF ERRORS

You can improve this manual by recommending improvements using DA Form 2928-2 located in the back of the manual. Simply tear out the self-addressed form, fill it out as shown on the sample, fold it where shown, and drop it in the mail.

If there are no blank DA Forms 2028-2 in the back of your manual, use the standard Form 2028 (Recommended Changes to Publications and Blank Forms) and forward to the Commander, Communications and Electronics Materiel Readiness Command, ATTN: DRSEL-ME-MQ, Fort Monmouth, NJ 07703.

In either case a reply will be furnished direct to you.

List of Illustrations

LIST OF TABLES

CHAPTER 1

INTRODUCTION

1-1. Scope

a. This manual contains direct support maintenance instructions for Test Set Group, Indicator, Radar OQ-63A/APS-94D. This manual includes instructions appropriate to direct support maintenance facilities for troubleshooting, testing aligning, and repairing the equipment. It also lists tools and test equipment required for maintenance.

b. The complete technical manual for this equipment includes TM 11-6625-1833-12.

1-2. Indexes of Publications

a. DA Pam 310-4. Refer to the latest issue of DA Pam 310-4 to determine whether there are new editions, changes or additional publications pertaining to the equipment.

b. DA Pam 310-7. Refer to the latest issue of DA Pam 310-7 to determine whether there are any modification work orders to the equipment.

1-3. Forms and Records

a. Reports of Maintenance and Unsatisfactory Equipment. Maintenance forms, records, and reports which are to be used by maintenance personnel at all maintenance levels are listed in and prescribed by TM 38-750.

b. Report of Packaging and Handling Deficiencies. Fill out and forward DD Form 6 (Packaging Improvement Report) as prescribed in AR 700-58/NAVSUPINST 4030.29/AFR 71-13/MCO P4030.29A, and DSAR 4145.8.

c. Discrepancy in Shipment Report (DISREP) (SF 361). Fill out and forward Discrepancy in Shipment Report (DISREP) (SF 361) as prescribed in AR 55-38/NAVSUPINST 4610.33B/AFR 75-18/MCO P4610.19C and DLAR 4500.15.

1-4. Reporting Equipment Improvement Recommendations (EIR)

EIR's will be prepared using SF 368, Quality Deficiency Report. Instructions for preparing EIR's are provided in TM 38-750, The Army Maintenance Management System. EIR's should be mailed directly to Commander, US Army Communications and Electronics Materiel Readiness Command, ATTN: DRSEL-ME-MQ, Fort Monmouth, NJ 07703. A reply will be furnished directly to you.

1-5. Calibration

Refer to the calibration procedures given in paragraphs 3-41 through 3-43 of this technical manual and the calibration procedures given in TB 11-6625-1833-35-1.

CHAPTER 2

PRINCIPLES OF OPERATION

Section I. TEST SET GROUP, INDICATOR, RADAR OQ-63A/APS-94D, BLOCK DIAGRAM ANALYSIS

2-1. General

Test Set Group, Indicator, Radar OQ-63A/APS-94D (test set group) is a portable test set that permits bench testing, aligning, calibrating, and trouble-shooting of the unite and plug-in modules of Radar Surveillance Set AN/APS-94D cockpit complex (less Recorder-Processor-Viewer, Radar Mapping RO-495/U). The test set group components function together as a single operating unit through inter-connecting cables simulating signals and voltages required for Radar Surveillance Set AN/APS-94D operation and testing.

2-2. Overall System Function

Test set group generates the video information and sweep signals required to operate either the fixed target or moving target cathode-ray tubes, or the monitor crt of Recorder-Processor-Viewer RO-495/U. Through the use of test set group cabling, units of the cockpit complex are tested under dynamic conditions by substituting units electrically for corresponding circuitry in the test set group. Plug-in modules of the units are tested dynamically by physically substituting them for corresponding modules in the test set group. Paragraph 2-3 describes the basic crt sweep requirements of a radar indicating system as information that will help to understand the functional operation of the test set group. Paragraphs 2-4 through 2-14 discuss the major block diagram functions of the test set group. Detailed block diagram functions are discussed in section II of this chapter. Detailed circuit functions are discussed in sections III through IX of this chapter.

2-3. Radar Indicating System Crt Swoop Requirements.
(fig. 2-l)

In order to maintain a linear display of video information on the crt, horizontal and vertical sweep signals must produce constant-velocity traces. Further, the traces must remain in *focus over* their entire length to maintain resolution. Provisions are required to permit rotation of the trace in correspondence with selectable simulated drift angle inputs (fig. 2-l). A means must be provided to correlate sweep direction and starting and stopping points with selectable simulated antenna switching modes. In the AN/APS-94E right(R) antenna mode,

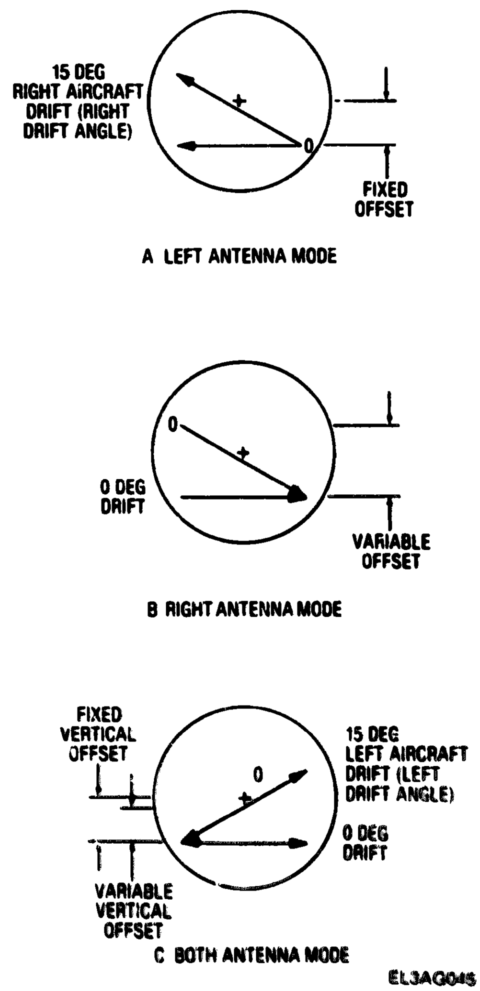


Figure 2-1. Crt sweep requirements.

the trace must start at the left edge of the crt and sweep right. In the left (L) antenna mode, the trace must start at the right edge of the crt and sweep left. In the BOTH antenna mode the trace must start at the center and sweep alternately in each direction in synchronism with antenna switching. Sweep rates must conform to selectable simulated range segments. Finally, vertical offset must be added to the sweep signals to meet crt photomapping requirements.

2-4. Video Simulator and Synchronizing Circuit

(fig. 2-2)

The video simulator and synchronizing circuit generates video information for display on the crt. In addition, this circuit generates the necessary timing signals for synchronizing the functions of other major circuits. The basic time reference for this circuit is a 5-MHz crystal controlled oscillator.

2-5. Sweep Circuit

(fig. 2-2)

The sweep control circuit contains circuitry for controlling rotation of the crt trace as well as selection of range display.

2-6. Horizontal Sweep Circuit

(fig. 2-2)

The horizontal sweep circuit contains circuitry necessary to generate a horizontal sweep ramp signal, offset this signal during left or right antenna mode, and correct the waveshape of the ramp signal to compensate for pincushion distortion. The ramp signal is also utilized by the vertical sweep circuit, the crt regulator and focus circuit, and the video amplifier.

2-7. Vertical Sweep Circuit

(fig. 2-2)

The vertical sweep circuit contains circuitry necessary to generate a vertical sweep ramp voltage in order to rotate the crt trace. The vertical sweep circuit also provides a fixed vertical offset. The ramp signal is also utilized by the crt regulator and focus circuit.

2-8. Video Amplifier

(fig. 2-2)

The video amplifier amplifies video signals from the video simulator and synchronizing circuit and provides fixed and selectable compression as a function of range display – antenna operation. The video amplifier also contains unblanking circuitry which receives a ramp signal from the horizontal sweep circuit.

2-9. Groundspeed/Drift Angle Servo Loop

(fig. 2-2)

The groundspeed/drift angle servo loop provides selectable channel operation. In the drift angle mode, a variable synchro input is supplied to a drift angle amplifier channel and is read out on a stepper-motor-

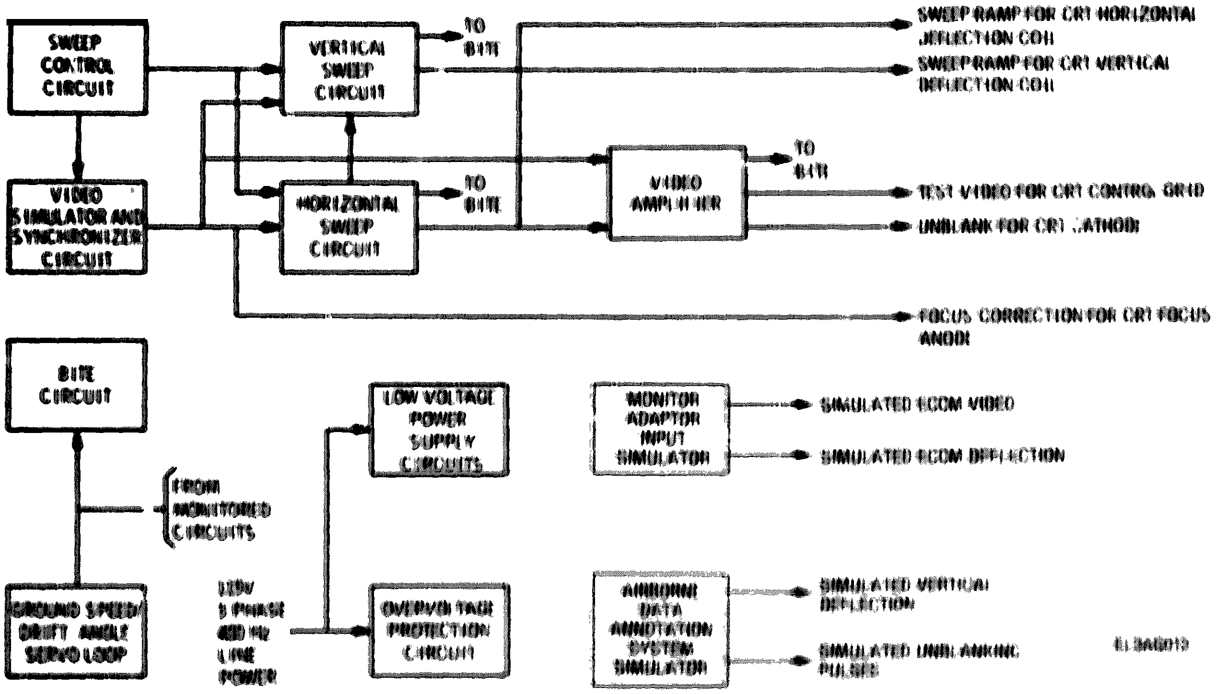


Figure 2-2. *Test Set Group, Indicator Radar [illegible] major functions block diagram.*

driven indicator. In the groundspeed mode, the same variable synchro input is supplied to a groundspeed amplifier channel and is read out on the same indicator. With the exception of a fault output to the BITE circuit and power source connections, the groundspeed/drift angle servo loop is independent of all other circuits in the test set group.

2-10. BITE Circuit
(fig. 2-2)

The BITE (built-in test equipment) circuit monitors major circuits in the test set group to provide four individual failure lamp indications. The vertical and horizontal sweep circuits and the video amplifier are monitored to provide failure indication on the first of the four lamps. The video amplifier is monitored to provide a sweep fault indication on the second lamp. The anode regulator and crt regulator and focus circuit are monitored to provide a fault indication on the third lamp. Either channel of the groundspeed/drift angle servo loop is monitored to provide a control fault indication on the fourth lamp.

2-11. Overvoltage Protection Circuit
(fig. 2-2)

The overvoltage protection circuit monitors each of the three phases of ac line power. At approximately 200 volts peak and above, the overvoltage protection circuit electronically short circuits each phase of line power, which is then interrupted by circuit breakers.

2-12. Low Voltage Power Supply Circuits
(fig. 2-2)

The low voltage power supply circuits provide 13 regulated voltages and one unregulated voltage. The voltages range from -20 vdc to +640 vdc.

2-13. Monitor Adapter Input Simulator
(fig. 2-2)

The monitor adapter input simulator generates simulated ECCM video and ECCM deflection signals. These signals are used to test the monitor display adapter circuits in Recorder-Processor-Viewer, Radar Mapping RO-495/U.

2-14. ADAS Simulator
(fig. 2-2)

The ADAS simulator provides vertical and unblanking signals to exercise the ADAS printer circuitry of Recorder-Processor-Viewer, Radar Mapping RO-495/U.

Section II. TEST SET GROUP, INDICATOR, RADAR OQ-63A/APS-94D DETAIL BLOCK DIAGRAM ANALYSIS

2-15. General

This section describes the functioning of the test set group at the detail block diagram level. All of the major circuits discussed in section I of this chapter are discussed on a detail block diagram basis. The sweep control circuit, vertical sweep circuit, horizontal sweep circuit, focus circuit, and the video amplifier, are included on one block diagram illustration due to the functional interrelationship of these circuits.

2-16. Video Simulator and Synchronizing Circuit
(fig. 2-3)

The video simulator and synchronizing circuit generates a basic time reference with a 5-MHz oscillator. The square wave output of the oscillator is supplied to a 750-Hz prf clocked counted and to the video amplifier circuit (para 2–32) through the pulse width logic circuitry. The 750-Hz prf clocked counter counts the 5-MHz square wave down to the 750-pulse repetition frequency (prf) used in the test set group. The output of the 750-Hz prf clocked counter is supplied to each of two groups of pulse width logic circuitry to establish pulse widths. One of the two groups of pulse width logic circuitry establishes the pulse width for the 750-Hz fixed-target (ft) video signal supplied to the video amplifier circuit. Pulse amplitude is controlled by VIDEO AMPLITUDE control 1A2R19. The other group of logic circuitry derives a sweep gate signal and a yoke clamp signal. The pulse width of these two signals is determined by control panel range selection. The third output from this group is supplied to a divide-by384 antenna counter. The output of the counter is supplied to a third group of logic circuitry that provides ft and moving-target (mt) enable pulses and an antenna gate. The antenna gate is selected by control panel selection for left, right, or both antenna operation.

2-17. Sweep Control Circuit-
(fig. FO-2 and FO-21)

The sweep control circuit provides control of antenna mode, horizontal and vertical range selection, and cathode ray tube (crt) trace rotation. Paragraphs 2–18 through 2–31 provide a description of the circuits that perform these operations. Figure FO–21 shows module interconnection for Test Set Subassembly MX–8639A/APS–94D (unit 2).

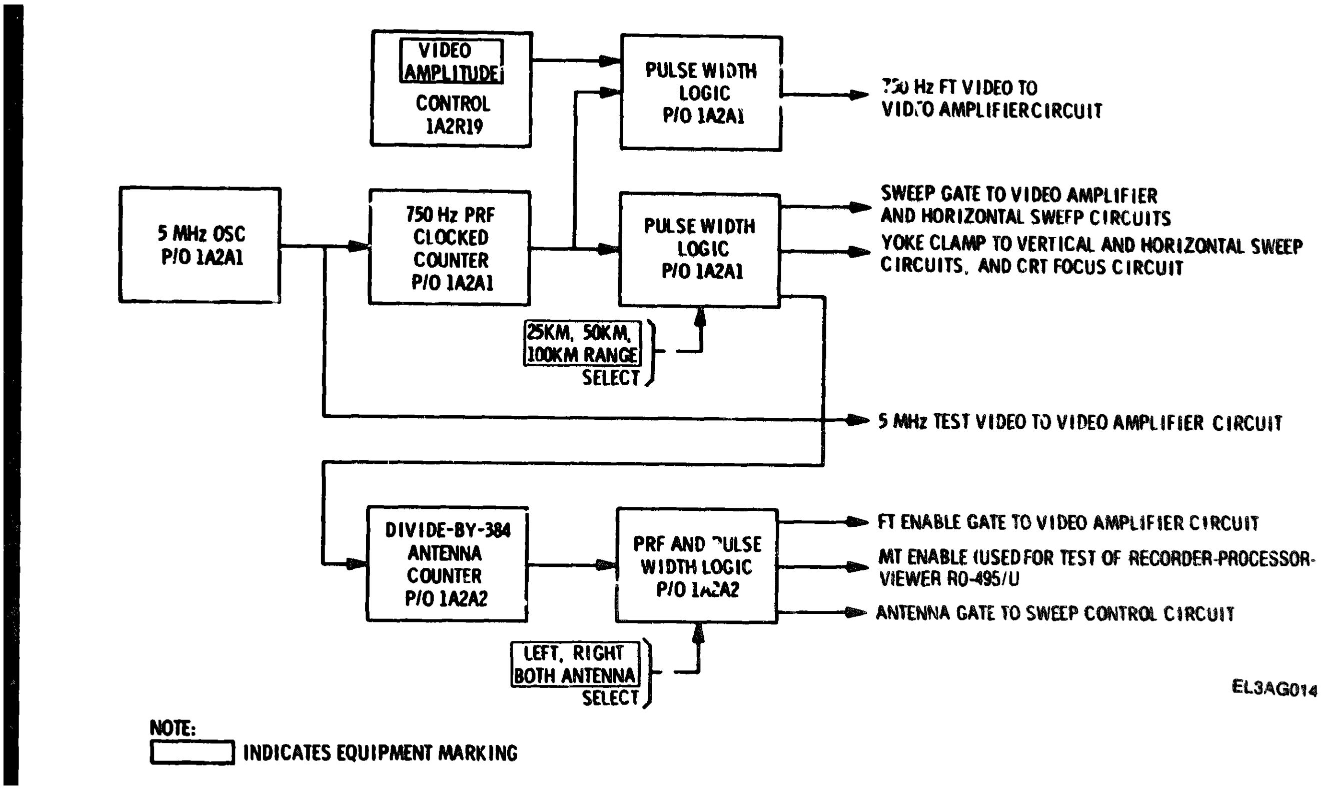


Figure 2-3. Video simulator and synchronizing circuits, block diagram

2-18. A Sine 0/ A Cosine 0 Signal Generation (fig. FO-2)

When ANTENNA switch 2S9 is set to either LEFT or RIGHT, the test set group operates in the single antenna mode. In this mode, the sweep control circuit receives from the video simulator and synchronizer circuit (fig. 2–3) an antenna gate that is either -4 volts (left antenna) or +4 volts (right antenna). When ANTENNA switch 2S9 is set to BOTH, the sweep control circuit receives a square wave antenna gate input from the video simulator and synchronizing circuit (waveform A fig. FO–2). The antenna gate is applied to left/right switch 2A1Q12, Q13 through switch driver 2A1Q10, Q11 via panel connectors and cables. When the antenna gate is +4 volts (right antenna) left/right switch 2A1Q12, 13 applies approximately +10 volts from 25 km right control 2TB3R5 to amplifier 2A6A1AR3, AR4. When the antenna gate is -4 volts (left antenna) left/right switch 2A1Q12, Q13 applies approximately -10 volts from OFFSET GAIN control 2R11 to amplifier 2A6A1AR3, AR4. The square wave outputs of amplifier 2A6A1AR3, AR4 are connected to cosine θ voltage divider 2A1R31, R32, R33, and sine voltage divider 2A1R28, R29, R30. The outputs of cosine voltage divider 2A1R31, R32, R33 are connected to DRIFT ANGLE switch 2S11 -3, -2. The outputs of sine voltage divider 2A1R28, R29, R30 are connected to DRIFT ANGLE switch 2S11, -9, -8. When DRIFT ANGLE switch 2S11 is set to 15, the voltage at wiper 2S11W3 represents the sine of 15 degrees and the voltage at wiper 2S11W1 represents the cosine of 15 degrees. Similarly, setting DRIFT ANGLE switch 2S11 to 1.8 enables the selection of voltages, from the cosine and sine voltage dividers, that represent the cosine and sine of 1.8 degree. Setting DRIFT ANGLE switch 2S11 to 0 connects wiper 2S11W3 to ground and connects wiper 2S11W1 directly to the output of amplifier 2A6A1AR4. (The signals at wipers W1 and W3 of DRIFT ANGLE switch 2S11 are termed A cosine θ and A sine θ, respectively, to distinguish them from cosine θ and sine θ signals developed through the action of the horizontal range selection circuit (para 2–19) and vertical range selection circuit para 2–20).) The A cosine θ and A sine θ signals at wipers W1 and W3 are coupled through source followers 2A6A1AR6 and AR2 to their respective sections of ANTENNA swtich 2S9 and to voltage dividers 2A7R11 — R14 and 2A7R7 — R10.

2-19. Horizontal Range Selection (fig. FO-2)

The A cosine θ signal is applied to horizontal range voltage divider 2A7R11 — R14 and ANTENNA switch 2S9B through source follower 2A6A1AR6.

Since the divider output is ultimately used as charging voltage for sweep generator 2A4A1AR2 in the horizontal sweep circuit (para 2-21), the slope of the horizontal sweep generator output ramp signal is controlled by selecting one of the horizontal range voltage divider outputs, providing 25, 50, or 100-km ranges. Selection of the proper divider output is accomplished by ANTENNA switch 2S9B in conjunction with RANGE switch 2S8B. The divider output is routed from wiper W4 of RANGE switch 2S8B through source follower 2A6A1AR5 to the horizontal sweep circuit as the cosine 0 signal. The cosine 0 signal developed here is applied to the horizontal sweep circuit (para 2-21 through 2-26) to generate signals necessary to modify the horizontal crt sweep when the trace is rotated 0 degrees.

2-20. Vertical Range Selection
(fig. FO-2)

The operation of the A sine 0 channel is similar to that of the A cosine 0 channel with two exceptions. First, there is no A sine 0 signal when DRIFT ANGLE switch 2S11 is set to 0 zero) because in that position wiper W3 is grounded. Second, an offset gain voltage is applied to the A sine 0 signal to provide control of the position of the trace on the crt. The offset gain signal is applied to the antenna gate by adjusting OFFSET GAIN control 2R11 (para 2-18). The A sine 0 output at 2S8B (W1) is routed through source follower 2A6A1AR1 to the vertical sweep circuit as the sine 0 signal. The sine 0 signal developed here is applied to the vertical sweep circuit (para 2-28 through 2-31) to generate the signals necessary to position and rotate the crt trace to an angle of 0 degrees.

2-21. Horizontal Sweep Circuit
(fig. FO-2)

The horizontal sweep circuit contains circuitry necessary to generate a horizontal sweep ramp voltage, offset this ramp signal for single antenna operation, and correct the waveshape of the ramp signal to compensate for pincushion distortion. In addition, the horizontal sweep signal is used by the crt focus circuit and the vertical sweep circuit. Paragraphs 2-22 through 2-26 describe the operation of the circuitry performing these functions.

2-22. Horizontal Offset
(fig. FO-2)

The horizontal sweep circuit receives sweep gate (waveform D fig. FO-2) and yoke clamp (waveform E) signals from the video simulator and synchronizing circuit (fig. 2-3). These signals, in conjunction with the cosine 0 output of the sweep control circuit, generate proper drive currents for the ft and mt crt horizontal yoke loads. When the test set group is operated in either the left or right antenna mode, the crt trace must be offset to start at one edge of the cathode ray tube, rather than at the center. Voltages necessary to provide these offsets are developed by LEFT HORIZONTAL OFFSET control 2R9 and RIGHT HORIZONTAL OFFSET control 2R12 (fig. FO-2). ANTENNA switch 2S9C (W4) selects the appropriate offset control output, routes it through switch 2A4A1Q5 to summing amplifier 2A4A1AR4. Summing amplifier 2A4A1AR4 sums the offset voltage with the output of horizontal sweep generator 2A4A1AR2. Considerable power is required to hold the trace at the edge of the crt. To avoid unnecessary power dissipation, the yoke clamp output *of* switch driver 2A4A1Q2 inhibits application of the offset voltage, except during the yoke clamp interval, by turning off switch 2A4A1Q5. (Waveforms D and E are shown for zero range delay operation.) When ANTENNA switch 2S9C (W4) is set to BOTH, ground is applied to switch 2A4A1Q5 which, in turn, causes the offset signal input to summing amplifier 2A4A1AR4 to become zero volts, thus allowing the sweep to start at the center of the crt.

2-23. Horizontal Sweep Generator
(fig. FO-2)

The cosine 0 output from the sweep control circuit is applied as charging voltage to sweep generator 2A4A1AR2 through switch 2A4A1Q3, Q4. When the sweep gate is present, switch 2A4A1Q3, Q4 is open, allowing the sweep generator to develop a linear ramp output voltage (waveform F). At the end of the sweep gate, switch 2A4A1Q3, Q4 conducts to terminate the sweep. Since the yoke clamp terminates at the end of the sweep interval, the blanked trace returns to the center of the crt. When ANTENNA switch 2S9 is set to BOTH, the polarity of the cosine 0 signal revers with the antenna gate signal. This causes the sweep generator to provide a group of positive ramp signal outputs (left antenna), followed by a group of negative ramp signal outputs (right antenna). Before the sweep is supplied for the ft or mt deflection yoke loads, it must be corrected for pincushion distortion.

***2-24. Horizontal Pincushion* Correction**
(fig. FO-2)

Pincushion distortion results from the fact that the position of the spot on the face of the crt is not directly proportional to the deflection angle. In addition, spot deflection is not linear with respect to deflection yoke current. To compensate for these conditions, the output waveshape of horizontal sweep generator 2A4A1AR2 is altered to provide the proper yoke current waveshape. The deflection angle is linearly related to the arc sine of the horizontal and vertical yoke currents, and the position of the spot on the face of the crt is linearly related to the tangent *of* the deflection angle. Horizontal sweep generator 2A4A1AR2 and vertical sweep generator 2A4A1AR6 provide sweep signals that are linear with respect to time. Without correction, therefore, the spot would accelerate as it moved away from the center of the crt. By changing the waveshape of the horizontal and vertical sweep generator outputs, a composite yoke current is obtained so that spot deflection is related to the sine of the uncorrected deflection angle. This results in a constant spot velocity to assure linear display of information on the crt. Cubing amplifier 2A4A2AR9 and summing amplifier 2A4A2AR12 perform the correcting function for the horizontal sweep circuit. The cubing amplifier consists of a nonlinear network and an operational amplifier that generates an output which corresponds to the cube of its input divided by 100; or $E_{out} = \frac{(E_{in})^3}{100}$. This output is waveform G. This signal is combined with the offset sweep generator output from summing amplifier 2A4AlAR4 (para 2-22) by summing amplifier 2A4A2ARl2. In summing amplifier 2A4A2AR12, the cubed input is divided by 22 and summed with the offset sweep generator output to obtain the corrected output signal (waveform H). This signal is supplied to polarity sensor driver 2AlAR1, dc amplifier 2A2, and HORIZONTAL AMPLIFIER SWEEP LENGTH control 2R3.

2-25. Horizontal Yoke Loads
(fig. FO-2 and FO–22)

Dc amplifier 2A2 is a noninverting amplifier that supplies drive current for simulated mt crt horizontal yoke load lA2Ll or simulated ft crt horizontal yoke load lA2L4. This amplifier receives a feedback sample of yoke load current to assure that the yoke current is following the corrected sweep voltage (waveform H). The output of dc amplifier 2A2 is supplied to either simulated mt crt horizontal yoke load lA2Ll *or* simulated ft crt horizontal yoke load lA2L4, depending on the position of DISPLAY switch 2S3. HORIZONTAL AMPLIFIER CENTER control 2R2 and HORIZONTAL AMPLIFIER SWEEP LENGTH control 2R3 permit control panel adjustment of horizontal sweep centering and sweep length, depending on the position of HORIZONTAL AMPLIFIER switch 2S2. The corrected sweep (waveform H) is also supplied to polarity sensor driver 2A1AR1 (fig. FO–22). This driver is an inverting, open loop operational amplifier that saturates or cuts off at microvolt input levels. The output of 2A1AR1 driver power switch 2A1Q3–Q6 via bipolar switch 2A1Q2. Switch 2A1Q2 is opened between sweeps by the yoke clamp gate (waveform E fig FO–2) via switch driver 2A1Q1. This ensures that switch 2A1Q3–Q6 does not conduct in the absence of signal input at 2A1AR1. Current pulses supplied to simulated mt crt horizontal yoke load 2R8 are of opposite polarity to those supplied to either load 1A2L1 or load 1A2L4. In this manner, the +20–volt and -20–volt power supplies operate into essentially similar load and regulation requirements as are present in the radar system.

2-26. Horizontal Unipolarizer
(fig. FO-2)

In addition to pincushion correction, compensation *for* incorrect focusing of the edges of the crt (astigmatism) is incorporated in the test set group. Since the required correction is related to the position of the spot on the crt face, samples *of* horizontal and vertical sweep signals are supplied to the crt regulator and focus circuit, which develops the necessary correction voltages. Before the horizontal sweep sample is routed to the crt regulator and focus circuit, it is modified by a unipolarizer circuit consisting of negative sweep detector 2A4A1AR5 and horizontal unipolarizer 2A4AlAR7. In both antenna operation, the antenna gate causes polarity reversal of the horizontal sweep signal (waveform J). This signal is supplied to negative sweep detector 2A4A1AR5 where positive sweeps are suppressed (waveform K). At unipolarizer 2A4A1AR7 the horizontal sweep signal is summed with the doubled negative sweep detector output and then inverted (waveform L). This signal is supplied to the crt regulator and focus circuit where it is used to develop center-to-edge focus correction. This signal (waveform L) is also supplied to the vertical sweep circuit where it is used in the development of vertical pincushion correction. During single antenna operation, the crt regulator and focus circuit require input signals for edge-to-edge focus correction. The unipolarizer circuit provides the proper horizontal output in the same manner as for both antenna operation. However, since its inputs are different, its outputs are different. Waveforms M, N, and Q illustrate unipolarizer signals for right antenna operation. Waveforms O, P, and Q show the same signals for left antenna operation.

2-27. Regulated Plus and Minus 9-Volt Source
(fig. FO-2)

The horizontal and vertical sweep circuits require balanced positive and negative voltage sources. These voltages are developed from the regulated +15 vdc input to the sweep circuits. The +15 volts is supplied to source follower 2A4A2AR1, which provides the +9 vdc output. The -9 volts output is produced by inverter 2A4A2AR3. Consequently, any change in the +9 vdc source causes a corresponding change in the -9 vdc source and balance is maintained.

2-28. Vertical Sweep Circuit (fig. FO-2)

The vertical sweep circuit provides a fixed vertical offset of the crt sweep and generates a vertical sweep ramp signal to permit rotation of the crt sweep. Paragraphs 2–29 through 2-31 describe this function.

2-29. Vertical Offset (fig. FO-2)

The vertical sweep circuit receives an inverted sweep gate signal from driver 2A4AlQl in the horizontal sweep circuit. This signal, in conjunction with the sine θ and offset gain outputs from the sweep control circuit, generate proper drive currents for the ft and mt vertical yoke loads. In the vertical sweep circuit, two offset signals are required. One is a fixed offset voltage (static offset) from VERTICAL OFFSET control 2R10 that establishes the vertical position for the start or stop of the horizontal sweep. In order to maintain this position during receipt of aircraft drift angle inputs, an offset gain voltage (dynamic offset) is summed with the static offset. The amplitude of the dynamic offset depends upon the setting of ANTENNA switch 2S9, DRIFT ANGLE switch 2S11, and RANGE switch 2S8. In the left antenna mode, with RANGE switch 2S8 set to 25 and DRIFT ANGLE switch 2S11 set to 15, the summed static and dynamic offsets pass through switch 2A4AlQ6 to appear as one input for summing amplifier 2A4AlAR8. The dynamic offset (offset gain signal) originates in the sweep control circuit and is supplied to polarity sensor 2A4A1AR1 and switch 2A4AlQ8. Polarity sensor 2A4AlARl turns on switch 2A4AlQ3, permitting the dynamic offset voltage to pass through low-pass filter 2A4AlC8, R18, and source follower 2A4AlAR3 in the presence of drift angle input. The output of 2A4AlAR3 is fed to summing network 2A4AlR4, R21 where it is summed with the static offset voltage (2R10), causing the spot position to shift point 0 (A, fig. 2-l). When the sweep gate occurs, the output of vertical sweep generator 2A4A1AR6 is applied to summing amplifier 2A4A1AR8 so that the spot traces the path shown. Setting ANTENNA switch 2S9 to RIGHT reverses polarity of the dynamic offset voltage. Polarity sensor 2A4A1AR1 turns switch 2A4A1Q8 off and turns 2A4A1Q7 on via ANTENNA switch 2S9D (W3). With switch 2A4A1Q7 on, a zero volt level is summed with the static offset signal. Consequently, the output from summing amplifier 2A4A1AR8 causes the trace to sweep down as shown at B, figure 2–1. In the BOTH antenna mode, -20 vdc is supplied to switch 2A4A1Q7 via ANTENNA switch 2S9D (W3) to hold this switch off. Since the polarity of the dynamic offset signal reverses in step with the antenna gate, switch 2A4AlQ8 is continuously toggled by the polarity sensor. With left aircraft drift (C, fig. 2-l), switch 2A4A1Q8 is on during the right antenna interval, charging capacitor 2A4A1C8 to the value established by voltage divider 2A7R7–R10 in the sweep control circuit. During the left antenna interval, switch 2A4A1Q8 is open; however, capacitor 2A4A1C8 holds its charge, and the dynamic offset is maintained at summing network 2A4A1R4, R21 so that the spot traces the path shown at C, figure 2–1. A vertical offset override signal can be supplied to switch 2A4A1Q6 to inhibit application of the vertical offset signals. This signal is provided by setting VERTICAL OFFSET OVERRIDE switch 1A2S4 to ON which allows approximately -20 vdc turn off potential to be applied to 2A4A1Q6 through load 2A4A1R11.

2-30. Vertical Sweep Generator. (fig. FO-2)

Sweep generator 2A4AlAR6 and switches 2A4AlQ9, Q10 operate in the same manner as the sweep generator circuitry in the horizontal sweep circuit. However, since the charging voltage is derived from the sine 0 output of the sweep control circuit, the output ramp of the sweep generator reverses with drift angle as well as antenna selection. The offset vertical sweep signal from summing amplifier 2A4AlAR8 is supplied to the pincushion correction circuit before being routed to the ft and mt vertical deflection yoke loads.

2-31. Vertical Pincushion Correction (fig. FO-2)

The conditions relating to pincushion distortion correction in the horizontal sweep circuit are applicable for the vertical sweep circuit. However, the vertical sweep circuit requires incorporation of the horizontal signal since vertical deflection is small with respect to horizontal deflection. Uncorrected vertical and horizontal sweep signals are combined in a multiplier circuit consisting of logarithmic amplifiers 2A4A2AR5, AR7, summing amplifier 2A4A2AR8, and antilogarithmic amplifier 2A4A2AR10. Prior to multiplication, the vertical sweep signal is fed to a unipolarizer circuit (negative sweep detector 2A4A2AR2 and vertical unipolarizer 2A4A2AR4) that performs the same function as the unipolarizer circuitry in the horizontal sweep circuit. Waveform S illustrates the unipolarized uncorrected vertical sweep signal for right antenna mode and either 1.8 or 15 degrees drift angle. The output from unipolarizer 2A4A2AR4 is supplied to summing amplifier 2A4A2AR8 through logarithmic amplifier 2A4A2AR5. The output of 2A4A2AR5 (waveform T) is a function of the logarithm of its input. The second input to summing amplifier 2A4A2AR8 is the output of logarithmic amplifier 2A4A2AR7 (waveform U). This amplifier has a transfer function equivalent to $E_{out} = \log 1.6 (E_{in})^2$. Summing amplifier 2A4A2AR8 adds and inverts its inputs to provide an input for antilogarithmic amplifier 2A4A2AR10. This amplifier provides an output (waveform V) that is proportional to the antilogarithm of its input. Consequently, its output is proportional to the product of the horizontal and vertical sweep signals. A portion of this signal is summed in summing amplifier 2A4A2AR11 with the uncorrected vertical sweep voltage to produce the corrected vertical sweep (waveform W) for the vertical deflection yoke loads. Since the uncorrected sweep signal polarity can be positive or negative, the correction voltage must be inverted as required. This is accomplished by driver 2A4A2AR6, switches 2A4A2Q1 and 2A4A2Q2, and inverter 2A4A2AR13. When the uncorrected vertical sweep (waveform R) is negative, negative sweep detector 2A4A2AR2 provides a positive output that is inverted by driver 2A4A2AR6 to turn on switch 2A4A2Q1. With 2A4A2Q1 on, the direct output of the antilogarithmic amplifier passes through the switch. When the uncorrected sweep is positive, negative sweep detector 2A4A2AR2 develops a negative output and switch 2A4A2Q2 is turned on, causing the inverted correction signal from inverter 2A4A2AR13 to pass through switch 2A4A2Q2. The selected output is routed through voltage divider 2A4A2R62, R63, R75, R76 to summing amplifier 2A4A2AR11 where it is summed with the uncorrected sweep signal. The corrected sweep output (waveform W) from summing amplifier 2A4A2AR11 is fed to dc amplifier 2A3 and to VERTICAL AMPLIFIER SWEEP LENGTH control 2R5. (Paragraph 2-41 describes operation of the dc amplifiers). In addition to corrected sweep output, the vertical sweep circuit provides a unipolarized output signal for use by the crt regulator and focus circuit.

2-32. Video Amplifier Circuit (fig. FO-20)

The video amplifier circuit receives video from the video simulator and synchronizing circuit (fig. 2-3), prepares this information for display, and supplies it to panel connector 2J1. Two video signals are supplied to the video amplifier; an ft video signal that is a 102.4 µs pulse at 750 Hz and a test video signal that is a 5-MHz square wave. Video signal selection is accomplished by setting TEST VIDEO switch 1A2S3 to ON for test video or to OFF for ft video. In the ON position, +28 vdc is supplied to the solenoid of relay 1A2K4 through TEST VIDEO switch 1A2S3. In the OFF position, ft video is applied to video amplitude adjust potentiometer 1A2A6A2R2. VIDEO AMPLITUDE control 1A2R19 (fig. 2-3) provides front-panel control of the ft video input level. The amplified video output of emitter follower 1A2A6A2Q4 is supplied to fixed compressor 1A2A6A2CR3. This compressor reduces the gain of amplifier 1A2A6A2Q2, Q3 for large signal amplitude. The output of the fixed compressor is amplified by 1A2A6A2Q5, Q6 and supplied to selectable compressor 1A2A6A2CR7, CR8, CR9 through emitter follower 1A2A6A2Q7. This compressor network consists of three compressors that are selected by combinations of ANTENNA switch 2S9 and RANGE switch 2S8 settings. Selectable compression is necessary since increased video amplitude is required as effective range decreases or crt sweep speed increases. Example of a selected compressor: With RANGE switch 2S8A set to 50 and ANTENNA switch 2S9A set to either RIGHT or LEFT the following occurs. A ground is applied to the 50 position (contact 11) of switch 2S8A. This ground is coupled through W4 of 2S8A to ANTENNA switch 2S9A, contact 7 or 9 depending on whether LEFT or RIGHT is selected. The ground is coupled through W3 of switch 2S9A, connectors 2J4, 2J3, 2J1, and 1A2J11 and activates compressor 1 (1A2A6A2CR7) of selectable compressor network 1A2A6A2CR7, CR8, CR9. As shown in table 2-1, only fixed compensation is introduced by the selection of single antenna mode, 25 km range, since this condition provides the highest sweep speed. The compensated video is routed through emitter follower 1A2A6A2Q8 to FT GAIN control 1A2R6. This control permits output gain adjustment of the video amplifier. The output of 1A2R6 is fed to output clamp 1A2A6A1CR11, which operates in conjunction with INTENSITY control 2R6 via DISPLAY switch 2S3 (W5) to establish the proper base level for the video information. A fixed bias voltage is applied through load resistors 2A1R25 and R26, for ft video or mt video display, to output clamp 1A2A6A1CR11 and the contacts of DISPLAY switch 2S3 Varying INTENSITY control 2R6, with the DISPLAY switch in either FT or MT, varies the intensity of the video being displayed on the radar crt under test. The output from the clamp circuit is supplied to connector 1A2J1 for intensity modulation at the control grid of the radar crt when the latter is under test.

Table 2-1 Selectable Compressor Networks

ANTENNA switch position	RANGE switch position	Active compressor
RIGHT/LEFT	25 km	Fixed only
RIGHT/LEFT	50 km	CR7
BOTH	25 km	
RIGHT/LEFT	100 km	CR8
BOTH	50 km	
BOTH	100 km	CR8

2-33. Cathode Ray Tubing and Unblanking
(fig. FO-2)

Three operational inputs and one protective input are supplied to diode AND gate 1A2A6A1CR12, CR13, CR14, CR18. When any AND gate input is low, the gate is inhibited to provide crt blanking. The protection signal input (waveform AD) is a sample of the horizontal sweep circuit. This signal is supplied to operational amplifier 1A2A6A1AR1 through bipolar threshold detector 1A2A6A1CR19, CR20. Since one output of the detector is inverted and the other output is not inverted, amplifier 1A2A6A1AR1 develops a unipolar output (waveform AE). This output is supplied to switch 1A2A6A1Q9, holding this switch off. If a failure occurs in the horizontal sweep circuit, switch Q9 conducts to inhibit the diode AND gate and to provide a return for the SWEEP FAULT indicator lamp in the BITE circuit. The three inputs to the AND gate are the sweep gate (waveform AC) and ft enable gate (waveform Y) from the video simulator and synchronizing circuit (fig. 2-3), and +20 vdc through UNBLANK switch 1A2S6 The enable gate is high during single antenna operation. Consequently, unblanking is controlled by the sweep gate. In the both antenna mode, the enable gate inhibits the AND gate after each antenna gate transition. This permits unblanking to occur only during sweep gate intervals when the enable gate is high. When all inputs to the AND gate are high, switch lA2A6AlQ10 conducts to provide a ground for clamp lA2A6AlVR3. This clamp is a +31 vdc breakdown diode supplied by +100 vdc through OR gate lA2A6AlCR15, 16, When the ground return is removed from the clamp, its output rises toward +100 vdc, providing cutoff potential for crt cathode. In the event of failure in the +l00 vdc source, the diode OR gate supplied +28 vdc to maintain a safe cathode bias potential for the crt. Generation of unblank signals is prevented when UNBLANK switch 1A2S6 is in the OFF position.

2-34. Cathode Ray Tube Regulator and Focus Circuit

Static and dynamic focusing is required to maintain the spot on the crt face at a fixed shape and size Paragraphs 2-35 and 2-36 describe these circuits.

2-35. Static Focusing
(fig. FO-2)

Static focus is accomplished by a potentiometer that controls a focus module within the high voltage power supply in the RO-495/U

2-36. Dynamic Focus
(fig. FO-2)

Horizontal and vertical unipolarized sweep signals (waveforms S and Q) from the sweep circuits are supplied to a squaring circuit consisting of a nonlinear network and amplifier 244A1AR9 in a closed loop. The transfer function of this circuit is equal to the sum of the squares of its inputs or

$$E\ out = \frac{(E_1\ in)^2 + (E_2\ in)^2}{11.47}$$

2-37. Groundspeed/Drift Angle Servo Loop.
(fig. FO-3)

The groundspeed/drift angle servo loop consists of a servoamplifier stepper motor 2Bl, two gear trains, synchro control transformer lA2B1, synchro control transmitter 2B2, NAVIGATION switch 2S6, a NAV SIM control, and a GS/DFT control. The stator of control transmitter 2B2 develops 3-wire information that represents the angular displacement of its rotor with respect to a zero reference point (zero degrees drift angle). Excitation for 2B2 is 26 vac 400 Hz. The S-wire information is supplied to the stator of synchro control transformer lA2Bl through contacts of relay 1A2K6. The rotor of lA2Bl is either in a position of minimum inductive coupling (null) with the magnetic vector produced in its stator or displaced from null. When an error signal is induced in the rotor, it rotates away from the null position. The amplitude of the error signal is proportional to cosine 0, when 0 is the angular displacement of the rotor with respect to the magnetic vector. Any error signal output of lA2Bl is fed through switch 2A5A3Q7, Q8 to buffer 2A5A3AR5 via contacts of relay lA2K5 (restored). The error signal is either in-phase or out-of-phase with respect to the excitation voltage for 2B2, Consequently the error signal has a polarity as well as a magnitude characteristic. Switch 2A5A3Q5, amplifier 2A5A3Q6, and switch 2A5A3Q7, Q8 form a synchronous phase detector. The output of the detector is supplied to integrator 2A5A3AR6 through buffer 2A5A3AR5 (waveform B). Integrator 2A5A3AR6, positive and negative level detectors 2A5A3AR8, AR7; monostable multivibrator 2A5A2U8A, U12B, U8B; inverter 2A5A2U7C; and switch 2A5A3Q9-Qll form a variable prf generator. The integrator develops a positive or negative ramp output (waveform C) until the threshold of the applicable level detector is exceeded. Exceeding either threshold toggles multivibrator 2A5A2U8A, U12B, U8B which causes a negative transition to pass through inverter 2A5A2U7C to turn on switch 2A5A3Q9, Q10, Qll, which clamps the integrator input at ground This terminates the ramp, allowing the level detector output to return high (waveform D). As the error signal amplitude increases or decreases, the slope of the ramp voltage increases or decreases and, therefore, the time required to exceed the threshold level decreases or increases. Assume the error produces a series of negative ramp signals (waveform C), a train of negative pulses appears at the output of negative level detector 2A5A3AR8, causing a high level to be present at the output of cross-coupled gate U9A and a low-level at the output of cross-coupled gate U9B. These levels will remain until the error signal passes null and positive ramps are developed. During negative ramps the Q outputs of bistable multivibrators 2A5A2U11A and UllB control their steering inputs through comparators 2A5A2U9 and U10. During positive ramps the bistable multivibrators inputs are controlled by the bistable multivibrator Q outputs. Since the output of one bistable multivibrator controls the steering inputs to the other, the sequencing of their outputs are shown in waveforms G and H for a condition when the ramp signal passes through null from negative to positive ramps. Each comparator develops complementary output signals that are used as steering gates for the multivibrators. Toggling of the bistable multivibrators is accomplished by the signal from delay inverter 2A5A2U12A, U12C, U12D. This output is similar to the switch trigger (waveform F), except for a polarity reversal and a slight delay to prevent false triggering of the multivibrators. Waveforms G and H, and their complements, are supplied to drivers 2A5A2Q15-Q18 through inverters 2A5A2U7A, U7D, U7E, and U7F. Each driver provides a ground return for one winding of stepper motor 2Bl to enable that winding when the driver is on. At the occurrence of pulses from switch 2A5A2Q13, Q14, the enabled drivers conduct and supply drive current for two of the stepper motor windings causing the motor to rotate 45°. Waveform I through L illustrate the sequence in which the windings are activated, with brackets to indicate the change of sequence after passing through an error null. When a servo error exists, the error is coupled through amplifier 2A5AlQ7 and switch 2A5AlQ3, Q4 and Q5, as a servo fault to the BITE circuit (para 2-42).

2-38. Indicating System Low Voltage Power Supplies (Modules 1A1A3, A4) (fig. 2-4)

The indicating system low voltage power supplies provide power for the test set group indicating system circuits. Power transformer lAlT1 accepts the 3-phase input and converts it into six 3-phase outputs. Each of these outputs is rectified by a 3-phase bridge rectifier and supplied to a regulator circuit. One regulator circuit contains two shunt regulators while the remaining circuits contain series regulators. Since the operation of the series regulators is similar, only the -28 vdc regulator is discussed.

a. Minus 28-Volt *DC Regulator*. The unregulated output from 3-phase rectifier lAlA3AlCR19 through CR24 is filtered and supplied to series regulator lAlA3Ql. A sample of the regulated output is taken from a voltage adjustment potentiometer and compared with Zener diode reference voltage in differential error amplifier lAlA4AlQ3, Q2. The error signal is returned as control voltage to series regulator lAlA3Ql. Any change in the -28 vdc regulated output produces an error input for series regulator lAlA3Ql which compensates for the change. Although operation of the other series regulators is similar, it differs in that they do not have individual voltage adjustment potentiometers. Also, their regulated outputs are summed with the -28 vdc regulated level and compared with a ground reference. The plus and minus 15 vdc regulators use the regulated plus and minus 20 vdc as an input source.

b. *Shunt Regulators.* The output of bridge rectifier lAlA3AlCR13 through CR18 supplied two shunt regulator circuits. One circuit (lA1A3VR1, VR2) is a simple Zener diode regulator that provides +250 vdc for the dynamic focus circuit. The other shunt regulator provides +640 vdc for Recorder-Processor-Viewer, Radar Mapping RO-495/U. In this circuit an error signal is developed by comparing a sample of the regulated +531 vdc with the output of the -28 vdc regulator. The error signal controls shunt regulator lAlA4A2Q4, 1AlA3Q8 which compensates for output voltage variations.

2-39. Low Voltage Power Supplies (Module 1A2A3) (fig 2-5)

The power supplies on module lA2A3 supply power to monitoring and signal generating circuits in the test set group. Power transformer lA2T2 accepts the 3-phase input and converts it into three 3-phase outputs. Each of these outputs is rectified by a 3-phase rectifier and supplied to a regulator circuit. The unregulated output of 3-phase rectifier lA2A3CRl-CR6 is filtered and supplied to series regulator lA2A3Q9. A sample of regulated output is applied to error amplifier lA2A3Q7, Q8, and Q10 where it is compared with a Zener diode reference voltage. Any change in the regulated +28 vdc output produces an error signal which is amplified in the error amplifier. The error amplifier produces an output that causes the regulator to increase or decrease conduction to null the error. The error amplifier also contains short circuit switching (Q11) that turns off the regulator in the event of a short circuit at its output. Operation of the -5 vdc and +20 vdc regulators is similar, except that regulators lA2A3AR1, AR2 operate both as regulators and error amplifiers. Switch lA2A3Q12 and Q13 function as short circuit protectors Regulator lA2A3ARl is referenced to regulated +28 vdc The -5 vdc regulator performs in a similar manner, except that it uses differential

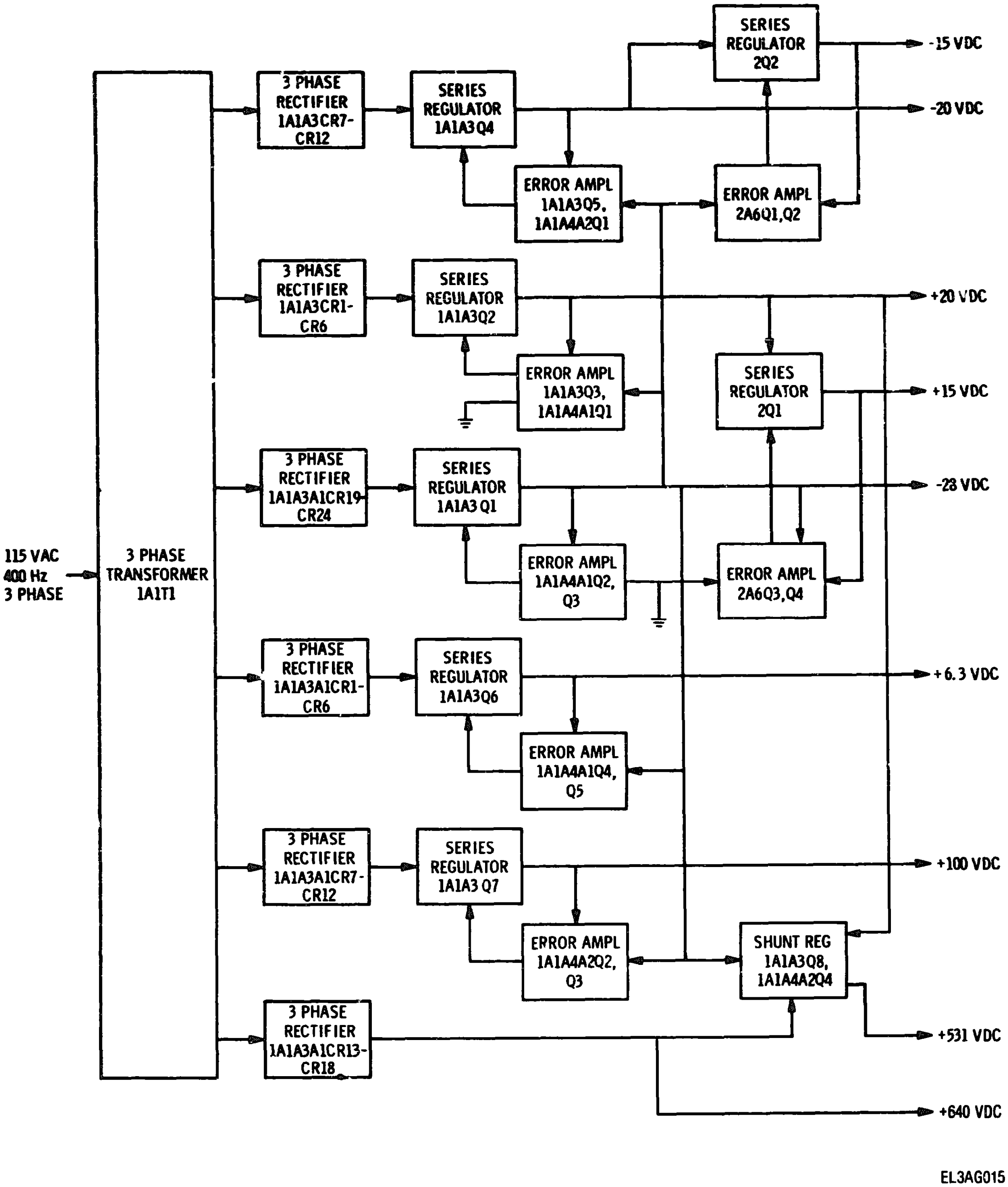


Figure 2-4. Indicating system low voltage power supply block diagram

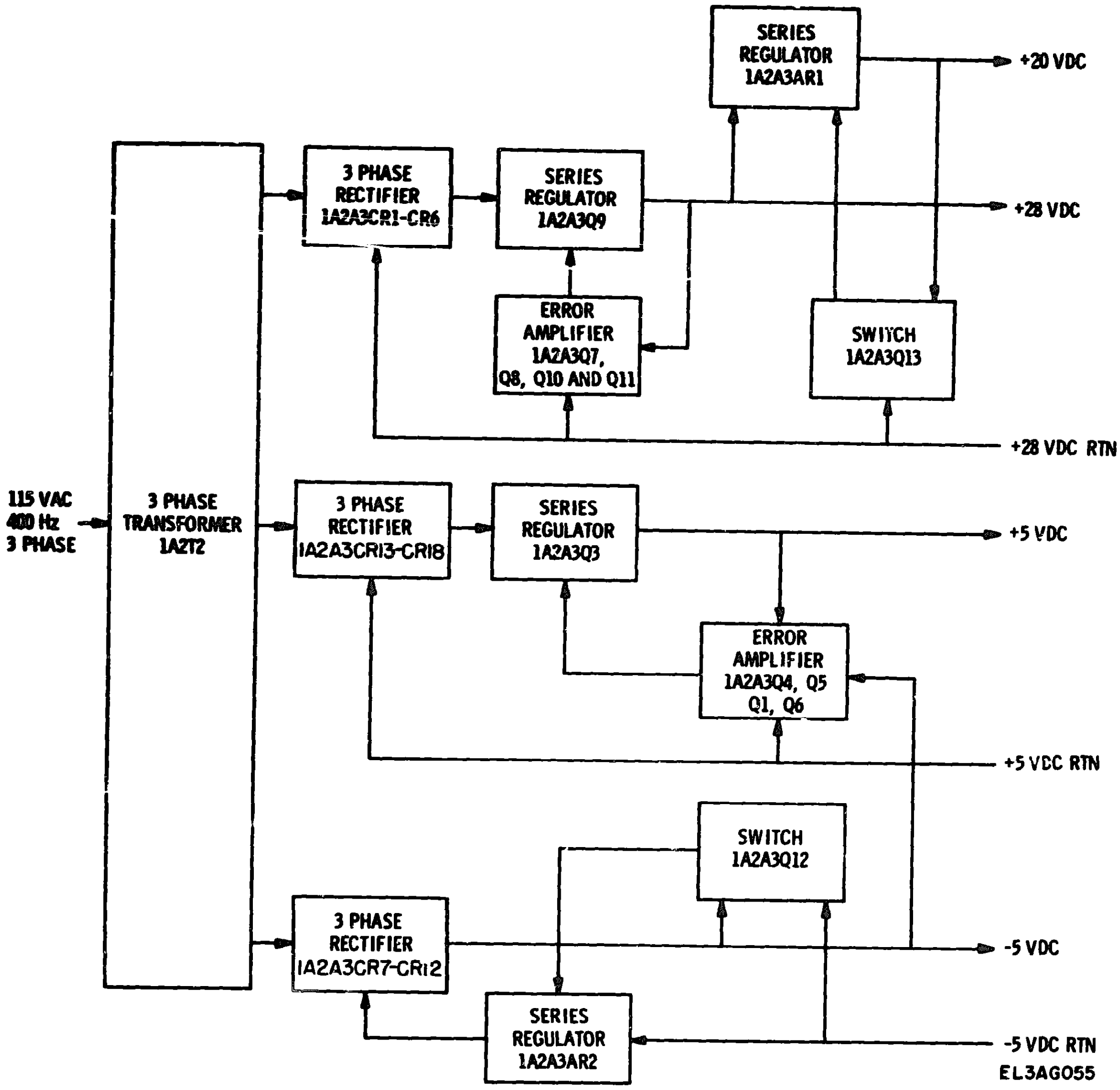


Figure 2-5. Low voltage power supply and regulator lA2A3, block diagram

amplifier lA2A3Q6 as the input to its error sensing circuit and is referenced to regulated -5 vdc. Switch lA2A3Q4 provides the short circuit, protection.

2-40. Overvoltage Protection Circuit
(fig. 2-6)

The overvoltage protection circuits for the 115-volt, 400 Hz, 3-phase supply consist of identical circuits for each of the three phases A, B and C. The following circuit analysis refers to phase-A circuitry by reference designation. When phase-A peak input voltage remains below approximately 200 vac, all switching componenta remain in their normally off state. When the positive excursions of phase-A peak input voltage rise above 200 vac, Zener diode lA2A5VRl conducts through CR1 (positive overvoltage sensor). Any overvoltage appears across voltage divider Rl and R2, causing switch driver Ql to supply the trigger potential at the gate of SCRQ2 (positive excursion grounding switch). With Q2 turned on, the positive excursion of phase-A Es effectively grounded. Near the end of the positive excursion, Q2 turns off and remains off until the occurrence of another overvoltage positive excursion. Capacitor Cl provides transient filtering to reduce the possibility of Q2 being triggered during other than overvoltage conditions. The negative excursion grounding circuit (SCRQ5) functions in the same manner, except for the opposite polarities involved and the addition of inverter lA2A5Q3 and Zener diode VR3 (threshold clamp). Q3 inverts the negative line excursions to provide a positive voltage for the base of switch driver Q4. Zener diode VR3 is used to increase trigg er stability at Q5 (negative excursion grounding switch).

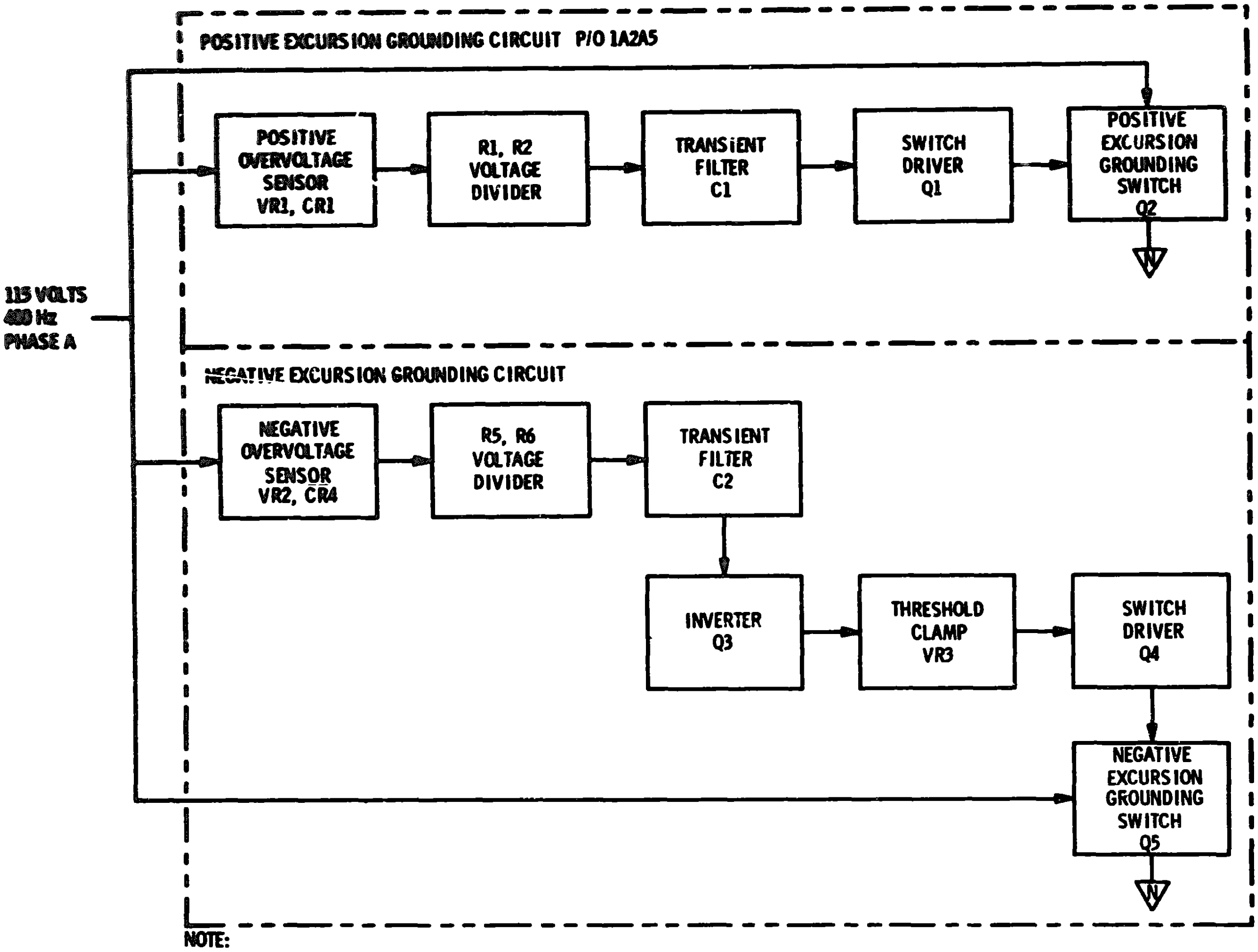


Figure 2-6. *Overvoltage protection circuit 1A2A5, block diagram*

2-41. Direct Current Amplifiers (fig. 2-7)

Two identical amplifiers are used to provide drive current for the ft and mt deflection yoke loads. External wiring permits the amplifiers to operate as inverting or noninverting amplifiers. An inverted output (2A3) is used to supply ft or mt vertical deflection yoke loads while a noninverting output (2A2) is used to supply ft or mt horizontal deflection yoke loads. The horizontal sweep signal from summing amplifier 2A4A2AR12 (fig. FQ-2) feeds dc amplifier 2A2 and the vertical sweep signal from summing amplifier 2A4A2AR11 (fig. FO-2) feeds dc amplifier 2A3. The amplifiers draw current from the +20 vdc supply and the -20 vdc supply. The dc amplifiers produce deflection yoke currents that retain the waveshape of the sweep signal input voltage. In amplifier 2A2 differential amplifier A1Ql (fig. 2-7) receives an offset voltage from centering potentiometer R9. Differential amplifier signal input is derived from the sweep signal and a feedback current sample from the deflection yoke load. The output of the differential amplifier is a voltage having a waveshape that will produce a yoke load current with the same shape as the sweep signal input. The output of the differential amplifier is inverted by A1Q2 and applied to complementary compound connected emitter followers Q3/AlQ7 and Q5/A1QS. The outputs of these emitter followers are supplied to complementary yoke drivers Q4 and Q6. The yoke drivers have common emitters with the deflection yoke load in the emitter circuit. Operation of dc amplifier 2A3 is essentially the same as 2A2 except that the sweep signal is supplied to the inverting input of the amplifier and the feedback signal is combined with the offset voltage.

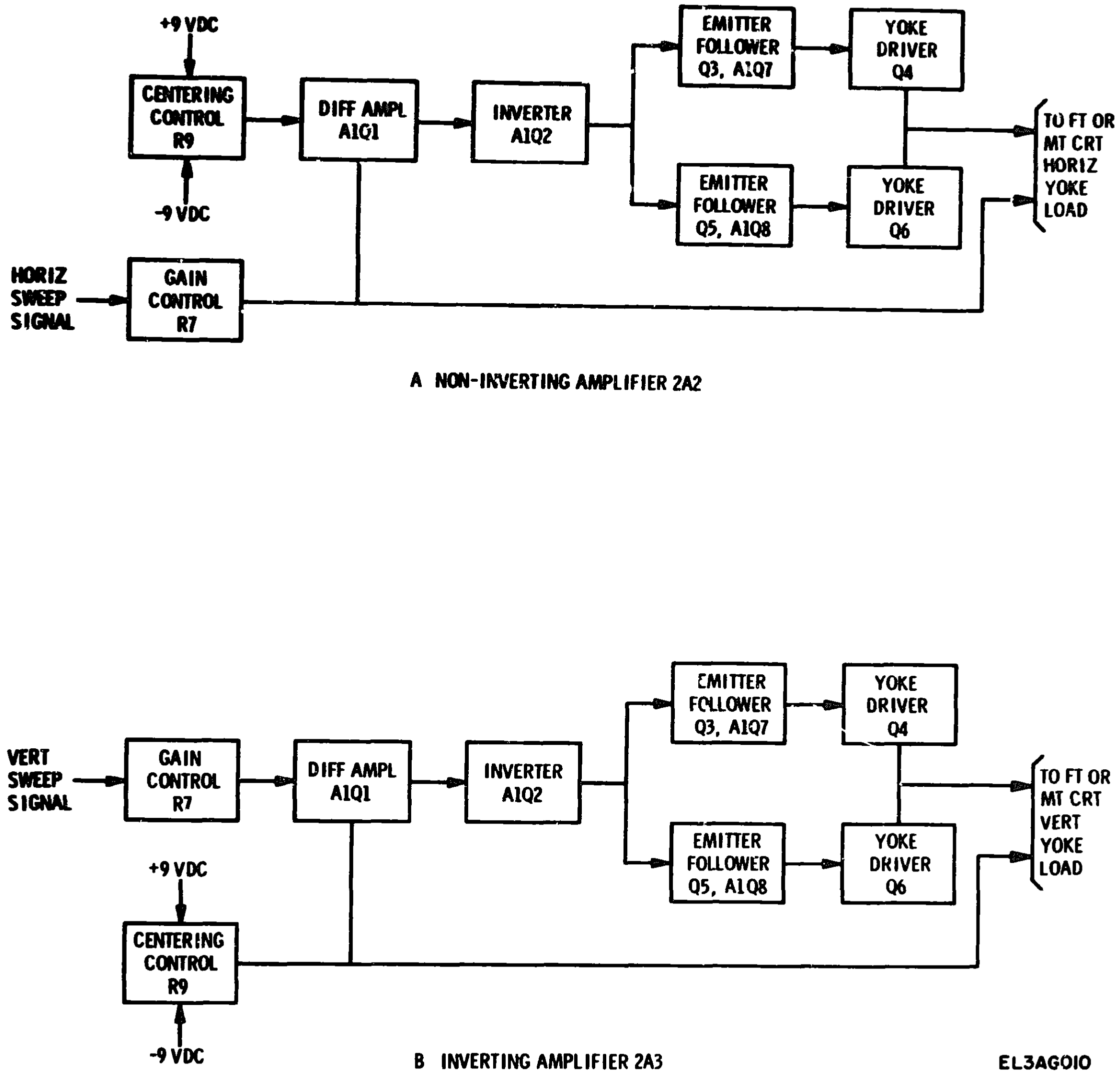


Figure 2-7. Direct current amplifiers 2A2/2A3, block diagram.

2-42. BITE Circuit
(fig. 2-8)

The BITE circuit consists of two major circuits; the primary fault detection circuit detects abnormally high or low voltages that may exist in the sweep waveforms (waveforms H and W, fig. FO-2), or in the video and unblank outputs of the video amplifier (fig. 2-3). Detected abnormalities in any of these waveforms cause FAILURE lamp lA2DS2 to turn on. The primary fault detection circuit is intended for use only during single antenna operation. Consequently normal as well as abnormal inputs are sensed as faults during both antenna operations. The fault isolation circuit functions on a go-no-go basis to indicate a malfunction in the sweep circuit, servoamplifier circuit, or the crt focus and regulator circuit.

Paragraph 2-43 discusses the primary fault detection circuit, and paragraph 2-44, the fault isolation circuit.

2-43. Primary Fault Detection Circuit
(fig. 2-8)

The primary fault detection circuit is enabled when BITE switch lA2S7 is positioned to ON. Because each of the four input circuits are similar, only the horizontal sweep input circuit is discussed. Horizontal sweep (waveform II, fig. FO-2) is applied to dual differential comparator lA2A4AR2 through closed loop operational amplifier lA2A4ARl (fig. 2-8). The comparator functions as a digital device whose output is normally low. If the peak-to-peak limits of the horizontal sweep waveform exceed the high or low

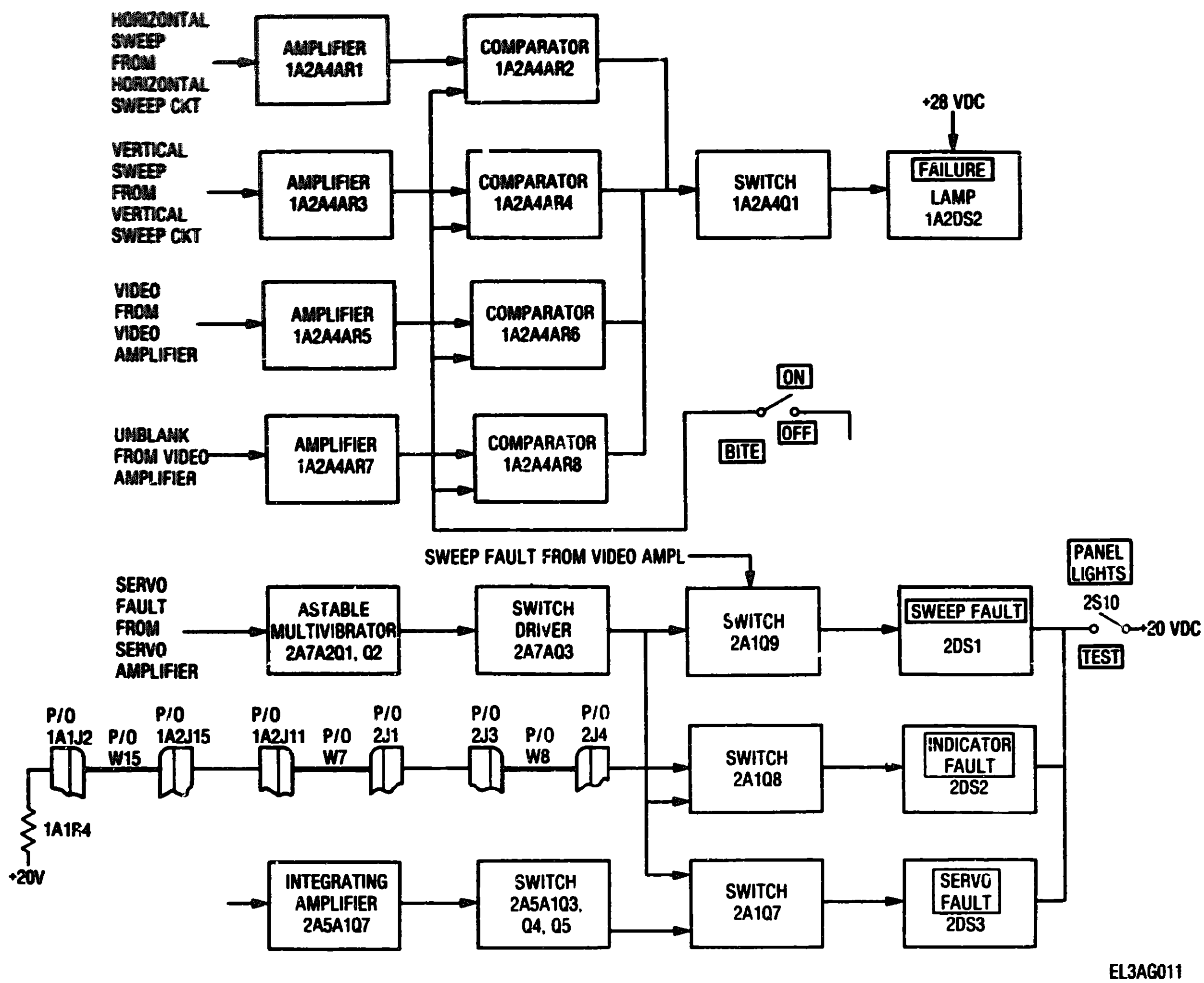


Figure 2-8. BITE circuit, block diagram

limits established by dc reference levels, the comparator output switches state from low to high. During normal input conditions, all comparator outputs are low and switch lA2A4Ql is off. However, at any time one or more comparators changes state, switch lA2A4Ql is turned on, which causes FAILURE lamp 1A2DS2 to turn on. Therefore, all input waveforms must be within their required voltage envelopes to hold the FAILURE lamp off.

2-44. Fault Isolation Circuit (fig. 2-8)

Astable multivibrator 2A7A2Q1, Q2 generates an asymmetrical rectangular pulse train that continuously toggles switch driver 2A7A2Q3 on and off. In the absence of normal sweep, servo, or high voltage BITE inputs, switch driver 2A7A2Q3 toggles switches 2A1Q7, Q8, Q9 through a control diode located at each switch input. When enabled, the toggled switches cause the SERVO FAULT, INDICATOR FAULT and SWEEP FAULT lamps to flash on and off in step with the astable multivibrator to indicate malfunction. However, with normal input, a control diode is turned off, isolating the affected switch from the switch driver, thereby turning off the related indicator lamp. The normal sweep input is supplied to the BITE circuit as a positive dc level. The servo fault signal is a variable prf pulse train (same as waveform F, fig. FO-3). The signal is inverted and filtered by amplifier 2A5A1Q7 to become a dc level that varies as a function of the pulse train prf. This dc signal is compared with a threshold level established by switch 2A5AlQ3, Q4, Q5. When the threshold is exceeded, the switch output is supplied to swtich 2AlQ7 as the enabling signal for the SERVO FAULT indicator. The INDICATOR FAULT signal in the OQ-63A is pulled to +20 vdc through lAlR4 which disables switch 2AlQ8. When checking the RO-495/U and there is an indicator fault (high voltage power supply failure), the indicator fault signal allows switch 2AlQ8 to be toggled by the astable multivibrator. PANEL LIGHTS TEST switch 2S10 permits indicator lamps 2DSl through 2DS3 to be checked for operation.

2-45. +28-Volt Regulated Power Supply and High Voltage Loads
(fig. 2-9)

Anode and focus voltages are divided down for measurement purposes in the networks associated with unity gain isolation amplifier Ul and U2. Rectifiers CR1 tbrough CR4 receive 43 vac and output +28 vdc unregulated. The unregulated voltage is routed through inductor Ll, in the 1Al panel assembly, and routed back to be regulated by Ql, Q2, VRl, and Q3.

2-46 +26-Volt DC Power Supply

The +26-volt power supply is a dc-to-dc supply that is sealed and non-repairable. Its input is +28 volts unregulated from the 1Al panel assembly. Its output is used to test the high voltage power supply in the RO-495/U.

2-47. ADAS Simulator
(fig. 2-10)

The ADAS simulator provides signals to exercise the ADAS printed circuitry of Recorder-Processor< Viewer, Radar Mapping RO-495/U. The simulator contains a programable read only memory which is programmed with BCD data equivalent to a complete ADAS data block. The simulator is started by a data demand pulse that originates in the RO-495/U. This pulse enables the clock generator. The clock pulses through a series of counters and decoders, control the reading of ADAS data from a series of counters and decoders, control the reading of ADAS data from a programable read only memory (PROM). The PROM outputs are routed through a data selector and a level shifter to provide unblanking signals for the RO-495/U. Vertical deflection signals are provided by a clock multivibrator and a deflection clock generator.

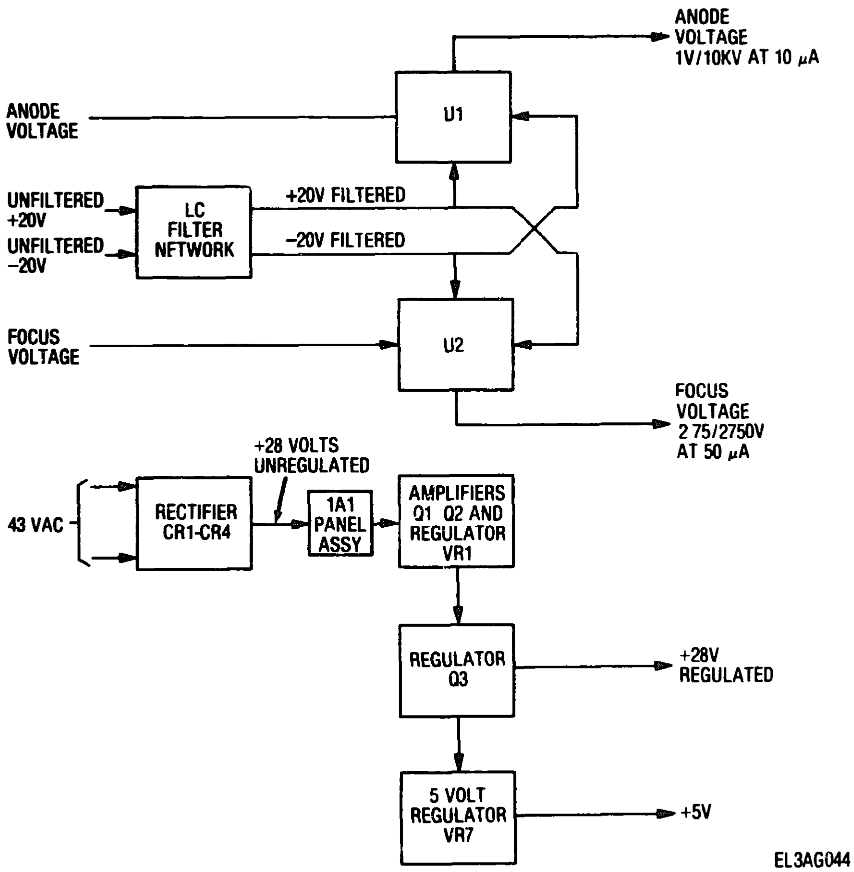


Figure 2-9. Regulated +28-volt power supply and high voltage loads, block diagram

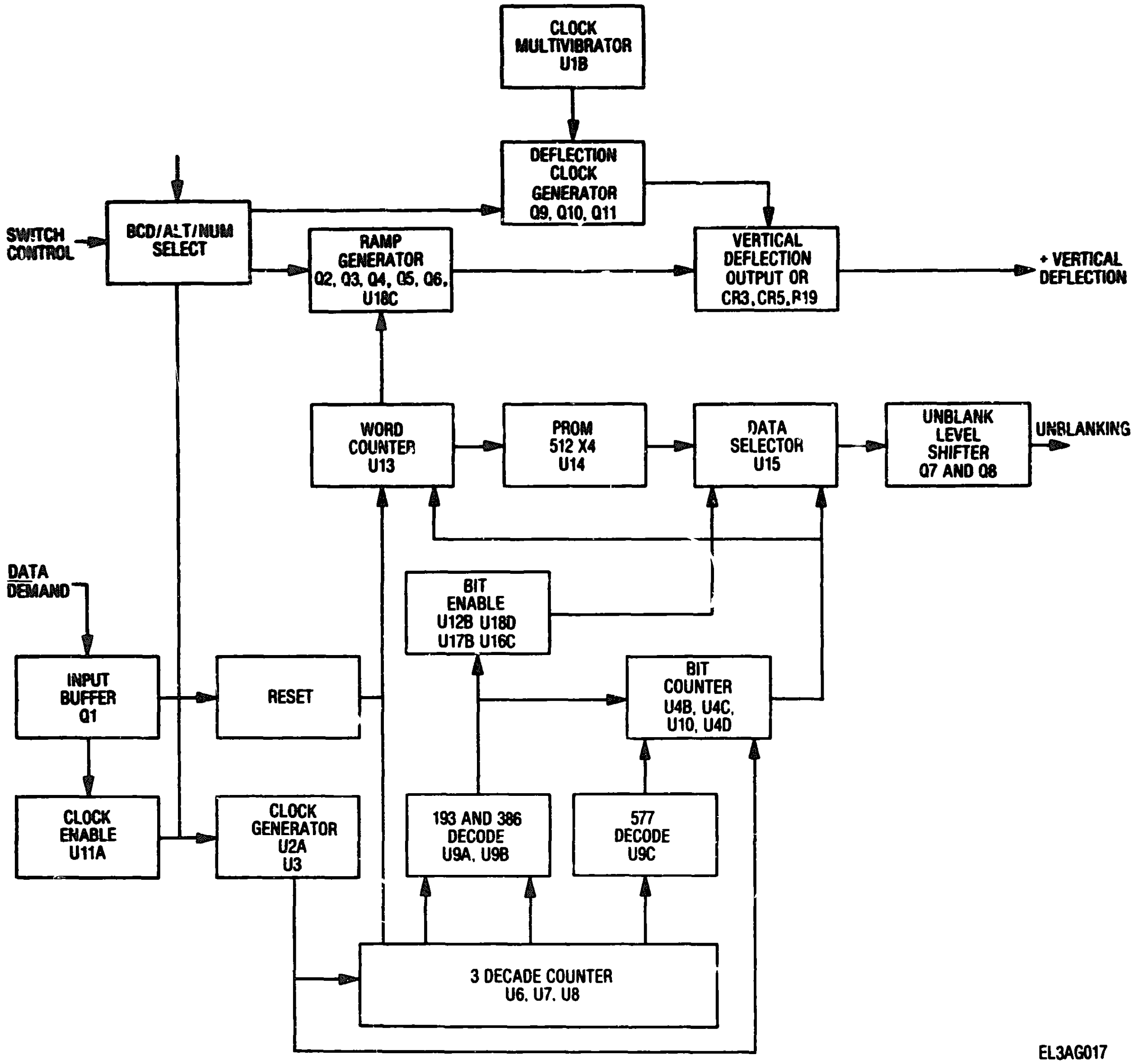


Figure 2-10. ADAS simulator circuit, block diagram

2-48. Monitor Adapter Input Simulator (fig. 2-11)

The monitor adapter input simulator provides signals to simulate system inputs to Recorder-Processor-Viewer, Radar Mapping RO–495/U. Circuit timing is controlled by a 4-flip flop binary counter, which is synchronized by a 13-khz clock. Binary counter count logic is used for gates decoding, in the generation of the ECCM video and the ECCM deflection signals. The count logic is also used to control the duration of a ramp voltage required for the generation of the ECCM deflection signal.

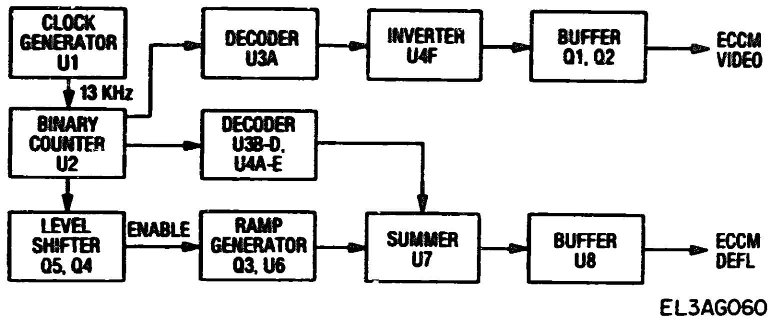


Figure 2-11. Monitor adapter input simulator, block diagram.

Section III. VIDEO SIMULATOR AND SYNCHRONIZING CIRCUITS, CIRCUIT ANALYSIS

2-49. General

Paragraphs 2-16 through 2-48 describe the functional operation of the test set group on a block dim level. This **section** covers the circuit analysis ***of*** stages in the video simulator and synchronizing circuits.

2-50. Video Simulator and Synchronizing Circuit

Paragraph 2-16 describes the functional operation, on a block diagram level, of the video simulator and synchronizing circuit. Paragraphs 2-51 through 2-60 provide detailed analysis of stage functioning in this circuit. Circuits covered are as follows: 5-MHz oscillator, 750-Hz prf clocked counter, 750-Hz prf generation, reset pulse generation, test video generation, sweep gate generation, yoke clamp gate generation, antenna counter, ft enable, and mt enable circuits.

2-51. Five-MHz Oscillator (fig. FO-15 and 2-12)

The basic time reference for the video simulator and synchronizer circuit is the 5-MHz oscillator consisting of amplifiers lA2AlU26A, U26C and 5-MHz crystal Yl (fig. FO-15). Amplifiers U26A, U26C are dual input NAND gates that function together as cascaded inverting square wave amplifiers. Regenerative feedback is peaked at 5 MHz by crystal Yl. Local negative feedback through resistor R2 stabilizes amplifier U26C. Local negative feedback through resistor R1 stabilizes amplifier U26A. Buffer U25A is a power NAND gate that provides load isolation. The 5-MHz square wave output of buffer U25A is supplied as the clock signal to a 13-stage counter chain. Buffer U25B provides additional load isolation and restoration of logic level for application to a line driver consisting of transistor driver lA2A4Q6 (fig. FO-18) and complementary emitter follower output stage lA2A4Q7, Q8. Capacitor lA2A4C28 improves lA2A4Q6 switching time by shunting clock pulse transitions directly to the base of Q6 for rapid charge and discharge of base-emitter capacitance. Diodes lA2A4CRl1, CR12 provide collector-base saturation clamping for improved turn off time of Q6. Additionally, diode CR11 provides required offset for stable turn off of Q6. Complementary emitter followers lA2A4Q7, Q8 improve output waveshape by providing symmetrical charge and discharge circuits for load capacitance. Resistor lA2A4R71 provides short circuit protection and resistor lA2A4R72 provides termination for coaxial transmission. Low-pass filters lA2A4L1, C33 and L2, C34 decouple high frequencies from the -5 vdc and +5 vdc supplies, respectively.

2-52. 750-Hz Prf Clocked Counter (fig. FO-15 and 2-12)

The 750-HZ prf utilized in the synchronizing circuit portion of the video simulator and synchronizer circuit is derived ***from*** the 5--MHz clock signal by a 13-stage clocked counter chain and associated logic circuitry. The binary elements of the clocked counter chain are dc clocked J-K flip-flops lA2AlU7, Ul through U6, U10 through U12, and U16 through U18. Clocking occurs at the positive transition of the clock pulse. Clock pulses are applied to the toggle (T) inputs. The dual J-K logic inputs Jl, J2 and Kl, K2 are enabled by logical “1” (2.6 vdc minimum). Therefore, unused J-K inputs are connected to +5 vdc. Complementary inputs J, K are enabled by logical “0” (0.40 vdc maximum). Therefore, unused complementary inputs are grounded. Set (S) and reset(R) inputs are activated by logical “0”. Because all set inputs are

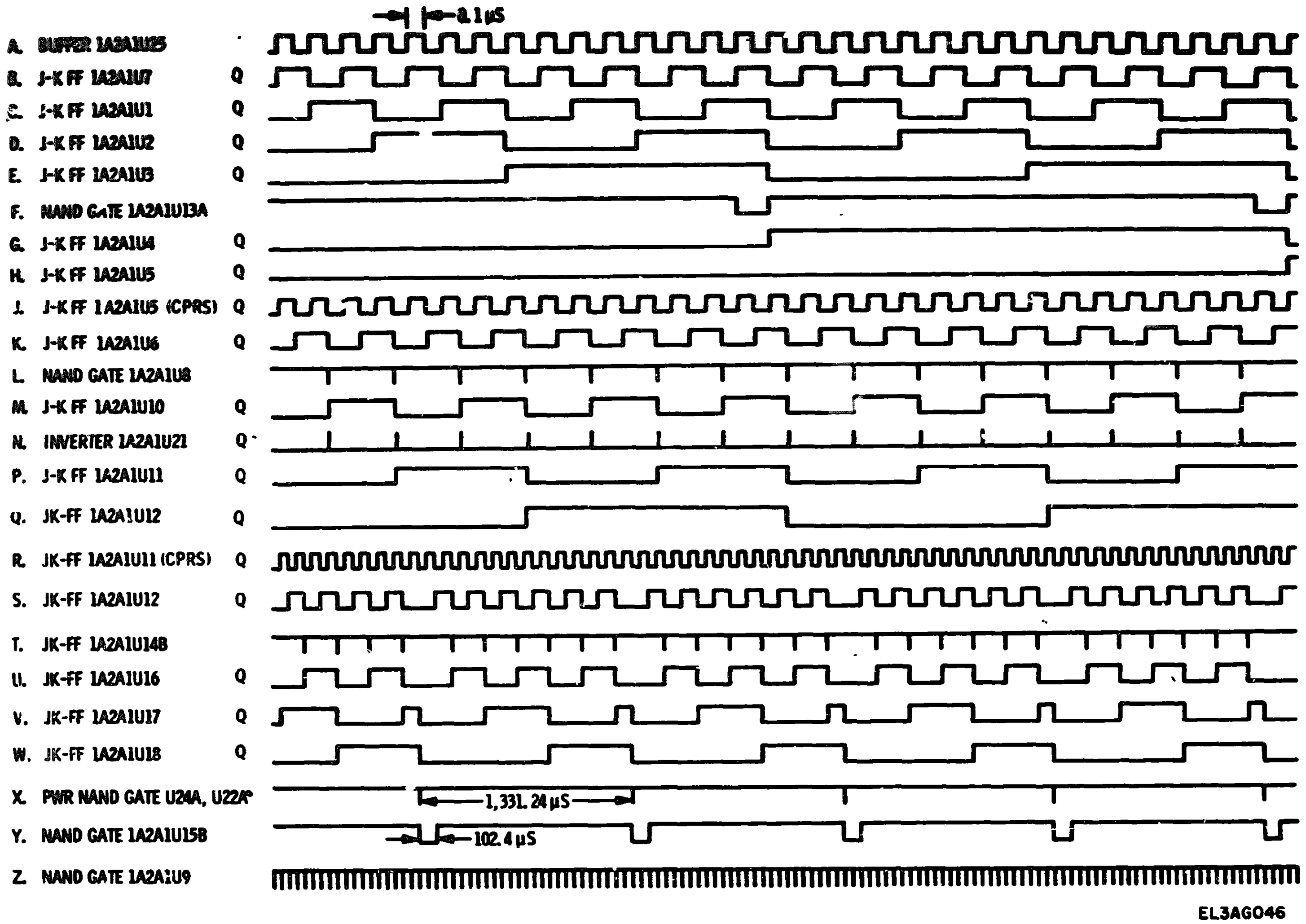


Figure 2-12. Timing diagram for Hz prf clocked counter (sheet 1 of 2)

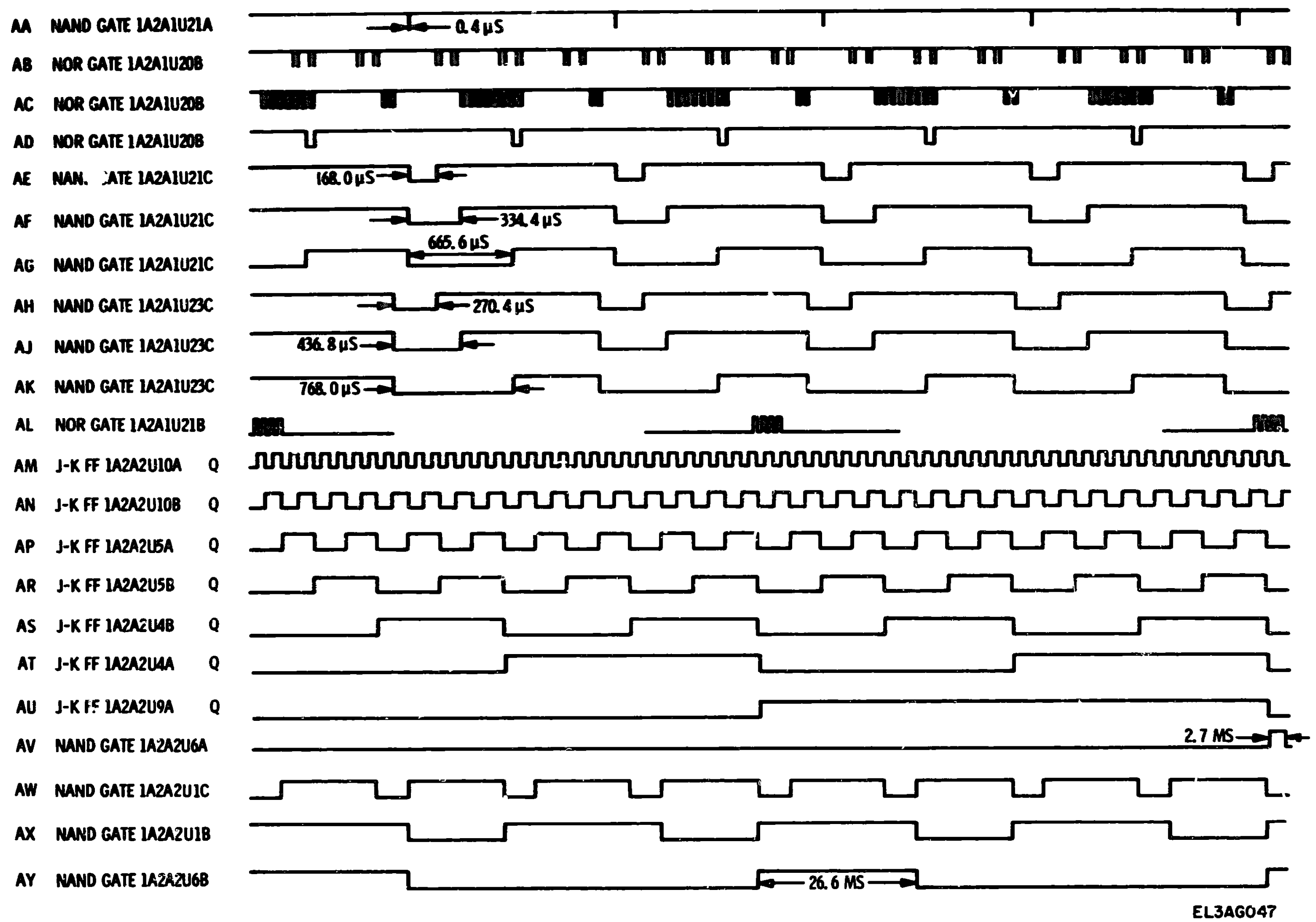


Figure 2-12. Timing diagram for 750 Hz prf clocked ***counter*** *(sheet* **2** *of 2)*

unused they are connected to +5 vdc. The truth table for the binary elements is given below.

Jn	Kn	Qn+1
0	0	Qn
1	0	1
0	1	0
1	1	Qn

Set	Reset	Q
0	0	+
1	0	0
0	1	1
1	1	Q

$J = J_1 . J2, \overline{J}$
$K = K_1 , K2, \overline{K}$
n is time prior to clock
n+1 is time following
+ both inputs in "0" state

The truth table above demonstrates that a toggle occurs only when all logic inputs are enabled and the set and reset inputs are not activated. The timing diagram for the 750-Hz prf clocked counter is shown in figure 2–12, waveforms A through W. Stable switching requires that logic levels are stable for a nanosecond period prior to and following clock pulse threshold voltage. Because the time scale of the timing diagram does not permit the illustration of such a short period, toggling will appear to occur, in many instances, during a logic level transition. Consequently it should be understood that phase separation exists between clock pulse transition (leading) and logic input transition (lagging) owing to propagation and parasitic delays.

2-53. 750-Hz Prf Generation
(fig. FO-15 and 2-12)

Each of the 13 stages of the clocked counter chain performs the divide-by-two function to provide the submultiples required for prf generation. NAND gate lA2AlU24A adds the Q output of flip-flops U12, U17, and U18 to generate a clock counter reset trigger pulse that occurs at the desired prf rate. The Q output of U12 is supplied to NAND gate U24A through externally connected pins J and W of lA2Al socket. The clock pulse is also supplied to U24A and to R-S flip flop U22 co establish reset pulse width. Assume that all stages of the counter are in the reset state (reset input is logic "0" or low, Q is logic "0" or low). The first positive transition of the clock pulse (waveform A, fig. 2-12) toggles flip-flop lA2AlU7 (fig. FO-15) whose logic inputs are connected to enable levels (ground or +5 vdc). The Q output of flip-flop U7 (waveform B inverted) enables the J-K inputs of flip flop Ul. With all logic inputs of flip-flop Ul enables, this stage toggles on the positive transition of the **clock** pulse (waveform C). In a similar manner each of the counter stages toggles on the first positive transition of the clock pulse to occur after enabling of logic inputs. The J-K inputs of flip-flops **U4** through U6 are enabled by adding the Q outputs of flip-flops U7, Ul, U2 and U3. This function is performed by NAND gate U13A (waveform F) NAND gate U8 adds the Q outputs (waveform L) of all stages preceding flip-flop U10 to provide $\overline{J}-\overline{K}$ enable inputs for stages U10 through U12. NAND gate U14B, in conjunction with NAND gates U8, U21 adds the outputs (waveform T) of all stages preceding flip-flop U16 to provide $\overline{J}-\overline{K}$ enable inputs for stages U16 through U18.

2-54. Reset Pulse Generation
(fig. FO-15)

NAND gate 1A2A1U24A adds the Q outputs of stages U12, U17, U18 and the inverted clock pulse output of NAND gate inverter U23B to provide the counter reset trigger pulse (waveform X, fig. 2–12). Because the narrowest pulse input to U24A is the clock pulse input, the output pulse width of U24A cannot exceed 0.1μs. The leading edge of this pulse occurs after the counter has counted 6656 clock pulses. This count is determined as follows. If the counter chain were not reset, it would perform the divide-by-8192 (2^{13}) function. That is, flip-flop U18 would complete one cycle for each 8192 clock pulses. However, the Q output of flip-flop U18 goes high at the end of (2^{12}). Further, the Q outputs of flip-flops U17 and U12 go high at counts 2048 (2^{11}) and 512 (2^9), respectively, following count 4096 of flip-flop U18. Consequently, at count 6656 ($2^{12} + 2^{11} + 2^9$), NAND gate U24A is enabled by the inverted clock pulse supplied from NAND gate inverter U23B. This pulse supplied through cross coupled NAND gates (R-S flip-flop) U22A, U22B to provide the 0.1μs reset pulse (waveform X). This pulse resets all stages of the counter chain. Waveform W shows that the output of flip-flop U18 is not symmetrical. This is because of the occurrence **of** reset at a count that is not a binary power. Similarly, the waveforms of all stages whose count is not an even submultiple of count 6656 (waveforms S, U, V) are affected by reset. The prf of the reset pulse is the clock prf divided by the clock count at reset, or:

$$\text{Reset prf} = 5\,(10^6)/6656 = 751.17$$

Therefore, the clock counter chain provides the desired nominal prf of 750. R-S flip-flop U22 ensures stable reset of all counter stages by providing a reset pulse whose width (approximately 50 to 100 nanoseconds) is independent of the width of the trigger pulse supplied by U24A. Assume that the output level of U24A is high, which is the condition existing between reset periods. The first clock pulse to appear at the input of U22A is ineffective if the output level of U22A is high (set state). If the output level of U22A is low (reset state), the trailing edge (negative transition) of the first clock pulse sets the R-S flip-flop. Subsequent clock pulses are therefore ineffective. When the reset pulse trigger occurs at the output of U24A, a clock pulse is present at the input of U22A and the R-S flip-flop is reset. The output level at U22A remains low for the duration ***of*** the clock pulse at its input, irrespective of the output level at U24A. The R–S flip-flop is set at the negative transition of the clock pulse.

2-55. Test Video Generation
(fig. FO-15 and 2-12)

NAND gate 1A2A1U15B adds the Q outputs of flip-flops U16 through U18 (waveforms U, V, W inverted) and the Q output of flip-flop U12 to obtain a 102.4μs pulse (waveform Y, fig. 2–12). Pulse width is established by the Q output of flip-flop U12 (0.2 (2^{10-1}) μs = 102.4μs). Pulse timing with respect to reset (waveform X) is established by the $\overline{Q}$ outputs of U18 and U16. The pulse output of U15B is supplied to the line driver consisting of Q14, Q15. Diode CR5 provides offset for turn off of driver Q14. The base of emitter follower Q15 is connected to ground through external VIDEO AMPLITUDE variable resistor 1A2R19 (fig. FO–14).

2-56. Sweep Gate Generation
(fig. FO-15 and 2-12)

NAND gate 1A2A1U9 adds the $\overline{Q}$ outputs of flip-flops U1 through U6, U10, U11 (waveforms C, D, E, G, H, J, K, M, P inverted, fig. 2–12) to provide the negative-going 0.4μs wide pulse output shown by waveform Z. The leading edge of these pulses is time coincident with the Q output of flip-flop U11 (waveform R). The output of U9 is supplied to NAND gate U21A through NOR gate inverter U19A as positive pulses. The output of NAND gate U15B is supplied to NAND gate U21A as positive pulses through NOR gate inverter U20A. NAND gate U21A adds the inverted outputs of U9 and U15B to provide the negative 0.4μs wide pulses shown at waveform AA. The output of U21A is supplied to R–S flip-flop U21B, U21C. NOR gate U20B also supplies an input to U21B, U21C. The output of U20B is a function of the setting of RANGE switch 2S8C (fig. FO–21). Plus 20 vdc is supplied, through RANGE switch 2S8C, to pin 1A2A1–3 (25 kilometers), pin 1A2A1–D (50 kilometers) or pin 1A2A1–E (100 kilometers). With RANGE switch 2S8 set to 25, switch 1A2A1Q1 (fig. FO–15) turns on to provide an enable level for NOR gate 1A2A1U19D. Similarly, NOR gates U19C or U19B are enabled when RANGE switch 2S8 is set to 50 or 100, respectively. Capacitors C2, C3, or C4 reduce input switch transients. With NOR gate U19D enabled, NAND gate U13B adds the Q output of flip-flops U3, U6, U11, and U16 (waveforms E, K, P, U) to provide the output waveform shown by waveform AB. Each pulse of each pulse pair shown in waveform AB is actually a pulse cluster containing 1.6μs wide pulses established by the Q output of flip-flop U3. The time scale of the timing diagram does not permit the practical illustration of these 1.6μs wide pulses with respect to the times relating to the remaining inputs to NAND gate U13B. The significance of these pulses is their time relationship to the input to R–S flip-flop U21C, U21B supplied by NAND gate U21A (waveform AA). At the leading edge of the first 1.6μs wide pulse in waveform AB, R–S flip-flop U21C, U21B is set (U21C output is high). Further pulses in waveform AB are ineffective with the R–S flip-flop set. At the occurrence of the first negative pulse in waveform AA, the R–S flip-flop is reset as shown in waveform AE. The R–S flip-flop remains reset until the occurrence of the next 1.6μs wide pulse of waveform AB at which time it is set. Further pulses in waveform AB are ineffective with the R–S flip-flop set. With RANGE switch 2S8 (fig. FO–21) set to 50, NOR gate 1A2A1U19C (fig. FO–15) is enables (NOR gates U19D, U19B are inhibited). NAND gate U14A adds the Q output of flip-flops U3, U10, U17 (waveforms E, M, V) to provide the resulting waveforms AC (simplified) and AF. When RANGE switch 2S8 (fig. FO–21) is set to 100, NOR gate 1A2A1U19B (fig. FO–15) is enabled (NOR gates U19D, U19C are inhibited). NAND gate U15A adds the Q outputs of flip-flops U11, U12, U16, U17 (waveforms P, S, U, V) to provide the resulting waveforms AD, AG. The output of U21C is supplied to line driver Q7, Q8, Q9. Diode CR2 provides required offset. Complementary emitter followers Q8, Q9 reduce pulse stretching induced by load capacitance. Resistor R19 inhibits oscillation of Q3, Q9. Resistor R21 provides short circuit protection. The output of U21B (waveform AE, AF, AG, inverted) is supplied to the antenna counter circuit (para 2-58).

2-57. Yoke Clamp Gate Generation
(fig. FO- 15 and 2-12)

R-S flip-flop lA2AlU23D, U23C is set (U23D output is **high) by** the first negative transition to appear at the output of NAND gate inverter U23A (same as waveform X). The set transition **of** the R-S flip-flop is shown in waveforms AH, AJ, AK. The next negative transition to appear at the output of NOR gate U20B (waveform AB, AC, or AD) causes the R-S flip-flop reset (waveforms AH, AJ, AK). The pulse output of the R-S flip-flop is supplied to line driver Q4, Q5, Q6 whose operation is identical to that for line driver Q7, Q8, Q9 (para 2-56). The yoke clamp gate is connected externally through pine U and 20.

2-58. Antenna Counter
(fig. FO-16 and 2-12)

The antenna counter divides the prf of the sweep **gate** to obtain the synchronized 5.9-Hz **square wave** antenna gate. Counting is performed by J-K flip-flops lA2A2U4, U5, U9A, and U10, which provide the divide-by-128 function. Consequently, the 751.17 prf of the sweep gate is counted down to the 5.9 Hz

(751.17/2") antenna gate frequency. The flip-flops in the antenna counter toggle at the negative transition of the toggle input. The reset input (R) is inhibited and the J–K inputs are enabled by connection to +5 vdc. The Q outputs of the counter stages are shown in waveforms AM through AU. Counter stages U5B and U8 are not used. NAND gate U1A is inhibited by the grounding of pin 1A2A2–V. The Q output of flip-flop U9A is supplied to NAND gate U7D. An inhibit or enable level is supplied to U7D by switch Q1 depending upon the position of ANTENNA switch 2S9C (fig. FO–21). With the ANTENNA switch set to LEFT, switch Q1 (fig. FO–16) turns on to supply an inhibit level to NAND gate U7D. With the ANTENNA switch set to BOTH or RIGHT, Q1 turns off to supply an enable level to U7D. Similarly, NAND gate U7A is inhibited or enabled by switch Q2 as a function of ANTENNA switch position. Consequently the Q output of flip-flop U9A is gated through U7D, U7A only when the ANTENNA switch is in BOTH position. In ANTENNA switch LEFT position, U7A provides a low output. In ANTENNA switch RIGHT position, U7A is inhibited to supply a high output. The output of U7A is supplied to line driver Q10, Q11, Q12 which functions in the same manner as line driver 1A2A1Q7, Q8, Q9 (para 2–56).

2-59. Ft. Enable

(fig. FO-16 and 2-12)

NAND gate 1A2A2U2 adds the Q outputs of flip-flops of U10B, U5A, U5B, U4B, U4A, enable outputs of Q1, Q2 (ANTENNA switch in BOTH position), and an enable output supplied by NAND gate U1D to provide the ft enable signal (waveform AV inverted). The output of U2 is inverted by NAND gate U6A, which is enabled by the inhibit output of NAND gate U1A. The output of U6A is supplied to line driver Q13, Q14, Q15 which functions in the same manner as line driver 1A2A1Q7, Q8, Q9 (para 2–56).

2-60. Mt Enable

(fig. FO-16 and 2-12)

NAND gate lA2A2UlC adds the Q output at flip-flops U5A and U5B to provide waveform AW. NAND gate U1B adds the output of U1C and the $\bar{Q}$ output of flip-flop U4B to provide waveform AX. NAND gate U6B adds the enable outputs of Q1 and Q2 (ANTENNA switch in BOTH position), the $\bar{Q}$ output of flip-flop U4A, and the output of UlB to provide the mt enable signal (waveform AY). This signal is inverted by NAND gate U7C and supplied to line driver *Q3*, Q4, *Q5*. This line driver functions in the same manner as line driver lA2AlQ7, Q8, Q9 (para *2-56).*

Section IV. HORIZONTAL AND VERTICAL SWEEP CIRCUITS, CIRCUIT ANALYSIS

2-61. General

The horizontal sweep circuits are shown on figure FO–2 and discussed functionally, on a block diagram level, in paragraphs 2–21 through 2–26. Paragraphs 2–62 through 2–65 describe the detail functions of the stages in this circuitry. Circuits discussed are as follows: sweep generation, cubing amplifier, negative sweep detector 2A4A1AR5 and unipolarizer A1AR7, and direct current amplifier 2A2. Vertical sweep circuits are shown on figure FO–2 and discussed functionally, on a block diagram level, in paragraphs 2–28 through 2–31. Paragraphs 2–67 through 2–72 describe the detail functions of the stages in this circuitry. Circuits discussed are as follows: sweep generation, negative sweep detector 2A4A2AR2 and unipolarizer A2AR4, logarithmic amplifier 2A4A2AR5 and A2AR7, threshold summing amplifier 2A4A2AR8 and antilogarithm amplifier A2AR10, vertical output switching, and direct current amplifier 2A3.

2-62. Sweep Generation

(fig. FO-24)

Horizontal sweep generator 2A4AlAR2 is gates *on* by a positive sweep gate signal from the video simulator and synchronizing circuit (fig. 2-3). When gated, the sweep generator provides a linear ramp output signal that is supplied to stunning amplifier AlAR4.

a. Sweep Gate Switches 2A4AlQ3, Q4. The sweep gate signal is capacitively coupled to switch driver 2A4A1Q1, inverted, and used to control two n-channel field effect transistor (fet) switches. Prior to the application of the sweep gate signal, switches AlQ3 and Q4 conduct to hold charging capacitor A1C7 near ground potential. Two switch networks are used since the conducting resistance of these switches is approximately 150 ohms. The cosine 0 signal, from the horizontal range selection circuit, is divided by 33 in voltage divider network AlR14, Q3 and then applied to voltage divider network R15, Q4 where it is again divided by 33. Thus, the input to sweep generator AR2 is effectively clamped at ground. During the interval of the sweep gate, switches AlQ3 and Q4 are cut off, allowing sweep generator AlAR2 to develop its output.

b. Sweep Generator *2A4AlR2 Sweep* generator 2A4AlAR2 is a hybrid module, operational amplifier connected as a bootstrap ramp generator that develops positive and negative output signals depending upon the polarity of the cosine 0 input signal. When switches AlQ3 and Q4 open, charging capacitor AlC7 charges toward the cosine 0 value through resistors A1R14, R15. Since sweep generator A1AR2 maintains a voltage null between its inputs, it develops an output with an amplitude that is twice that of the voltage appearing across the charging capacitor. This voltage is divided in half by feedback voltage divider A1R16, R19 and also returned to the charging capacitor through bootstrap resistor A1R17. As the exponential charging current through resistors A1R14, R15 and capacitor A1C7 decreases, the bootstrap current through resistor A1R17 and capacitor A1C7 increases, causing a constant current to flow through the charging capacitor. With a constant current flowing through the capacitor, a linear ramp voltage appears across the capacitor and produces a linear ramp voltage of twice the amplitude at the output of sweep generator A1AR2.

c. Summing Amplifier 2A4A1AR4 Operation. Summing amplifier 2A4A1AR4 is a hybrid module, operational amplifier that combines an offset signal with the output of sweep generator A1AR2. The offset voltage is supplied to summing amplifier A1AR4 through switch A1Q5 upon application of the positive-going yoke clamp signal. This switch is a p-channel fet that is driven into conduction by the inverted yoke clamp signal from switch driver A1Q2. Depending upon the position of ANTENNA switch 2S9 and RANGE switch 2S8, a variable horizontal offset voltage is supplied from voltage divider 2A7R7–R14 (fig. FO–27). When the ANTENNA switch is set to BOTH, positive and negative ramp voltages from sweep generator A1AR2 are inverted by the summing amplifier A1AR4 and supplied to negative sweep detector A1AR5 and cubing amplifier A2AR9. Setting the ANTENNA switch to LEFT selects a voltage between +3 and +3.6 volts from LEFT HORIZONTAL OFFSET potentiometer 2R9 (fig. FO–21). This voltage and negative ramp voltages from the sweep generator are summed by the summing amplifier to produce positive-going ramps that start below ground. Alternatively, negative ramp voltages that start above ground are produced when the ANTENNA switch is set to RIGHT.

2-63. Cubing Amplifier.
(fig. FO-24 and 2-13)

Cubing amplifier 2A4A2AR9 modifies the offset, bipolar ramp voltage from summing amplifier AlAR4. The cubing amplifier is a hybrid module, operational amplifier having a resistor-diode voltage sensitive input network. Figure 2-13 illustrates the cubing amplifier in simplified form, assuming positive input ramp voltages. Resistor R_a can be substituted for the series-parallel combination of resistors A2R27, R28, *R32,* R33, R37 and R38 since diodes A2CR6, CR7, and CR8 are reverse biased for positive ramp input signals (fig. FO-24). A cubing amplifier voltage gain of -0.24 is established, therefore, by resistors A2R48 and R53 causing the output to increase from zero volt to -0.96 volt. With the input ramp between +4 and +6.2 volts, diode A2CR3 conducts and the parallel resistor A2R47 with R48 change the voltage gain of the amplifier to approximately -0.5. Network resistor values are selected to provide minimum effect at the output curve break points. At the second and third break points, (+6.2 and 7.7 volts), the voltage gain is increased to -0.74 and -1.0 respectively. The effect of this shaping is to produce an output voltage curve that approximates the cube of the input divided by 100. When the amplifier receives negative ramp voltages, this process is repeated, except that the positive series-parallel network remains passive and the negative network (fig. FO-24) is active. The cubed output is combined with the input ramp voltage in summing amplifier A2A412, through nonsymmetrical summing network A2R60, R61, to produce a horizontal sweep signal that contains 96 percent of the ramp voltage and *4* percent of the cubed output.

2-64. Negative Sweep Detector 2A4A1AR5 and Unipolarizer A1AR7
(fig. FO-24)

Negative sweep detector 2A4AlAR5 and unipolarizer AlAR7 operate together to develop negative-going ramp voltages regardless of the polarity of the offset ramp signals from summing amplifier AlAR4. Output signals from the unipolarizer are supplied to logarithmic amplifier A2AR7 and the squared summing amplifier AlAR9.

a. Negative Sweep ***Detector AlAR5.*** The negative sweep detector is a hybrid module, operational amplifier circuit that provides a positive-going ramp output when its input ramp signa1 is negative-going. Positive input ramp voltages produce a zero-volt output level. Degenerative feedback establishes an amplifier gain of one through one of two feedback resistors, AlR28 or R30. When the input is positive, diode A1CR5 conducts and resistor AlR30 acts as the feedback resistor. Since pin 1 of AlAR5 and AR7 is at a virtual ground, no current flows through resistors AlR28 and R29. Thus, the amplifier circuit output at the junction of these resistors is zero volt. When the input ramp signal is negative, diode AlCR4 conducts to switch resistor AlR28 into the circuit as the feedback resistor. This causes the negative sweep detector circuit to develop a positive-going ramp voltage output.

b. Unipolarizer A1AR7. The unipolarizer receives two inputs that depend upon the polarity of the negative sweep detector input. When this signal is a positive ramp voltage, output from the sweep detector is zero volt. Thus, resistors AlR27 and R36 establish a voltage gain of one for the Unipolarizer,

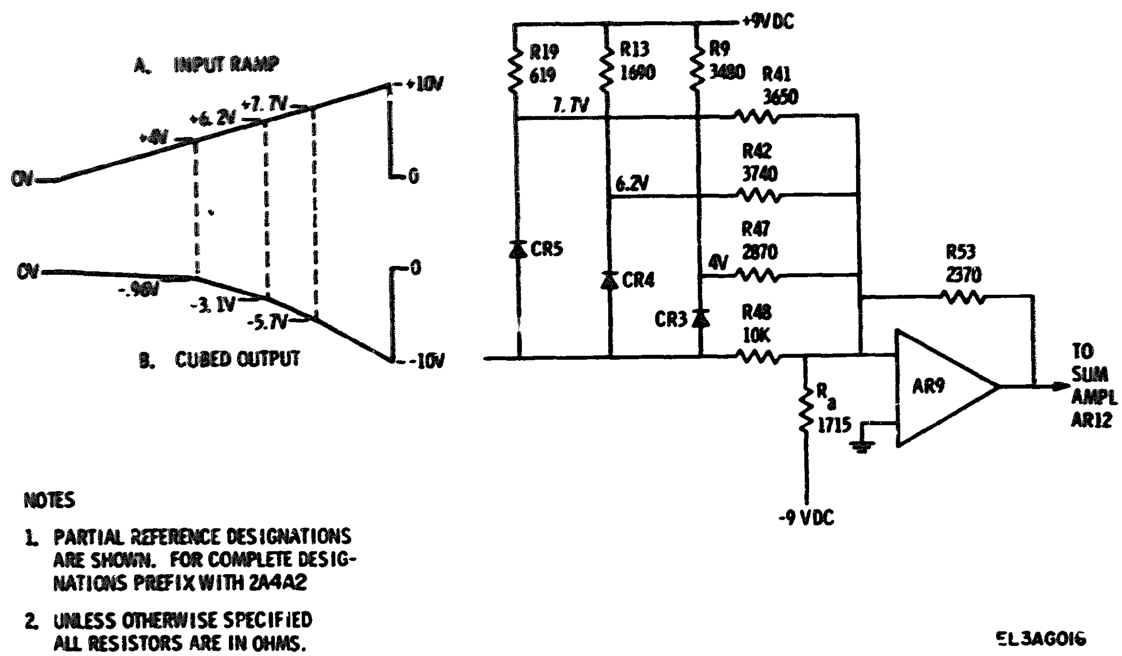


Figure 2-13. Cubing, amplifier, simplified schematic diagram.

causing its output to be a negative ramp signal having the same amplitude as its input. With a negative **ramp input to sweep detector AlAR5 positive and negative ramp voltages are combined in a summing network consisting** of resistors **AlR27 and R29. This** results in a negative ramp voltage output from uni-**polarizer** AlAR7 that has **the** same amplitude as the **negative** sweep detector input.

2-65. Direct Current Amplifier 2A2 (fig. FO-23)

Horizontal yoke currents for the ft and mt cathode ray tube deflection yokes are provided by dc amplifier module 2A2. Pincushion corrected horizontal sweep **sign**als from summing amplifier 2A4A2AR12 are supplied to the noninverting input of differential **amplifier 2A2A1Q1 through HORIZONTAL AMPLIFIER SWEEP LENGTH control 2R3 through HORIZONTAL AMPLIFIER switch 2S2. The inverting input to the differential amplifier is derived from HORIZONTAL AMPLIFIER CENTER control 2R2.** also through 2S2. The centering control is connected in a voltage circuit across ±9 vdc. The 9-volt sources **are developed by two Zener diode** regulators, 2AlVR3 **and VR4 (fig. FO–22). Amplifier** gain is controlled by **varying the length** control. The feedback to the is-**verting input is a sampie voltage through resistor 2A2A1R11 (fig. FO–23). This sample has the same wave shape as the deflection yoke current; thus, any deviation in yoke current wave shape from the input voltage waveform is corrected by altering the output voltage waveform from differential amplifier 2A2AlQl. The output from the differential amplifier is amplified by inverter 2A2A1Q2 and supplied to complementary, compound-connected emitter** followers 2A2AlQ7/Q3 and 2A2AlQ8/Q5. **In-phase outputs are taken from these emitter followers and supplied to a complementary push-pull power amplifier consisting** of transistors 2A2AlQ4 **and 2A2AlQ6. When the input sweep signal is at zero volt,** the output amplifier is balanced and no current flows in the ft or mt horizontal deflection yoke.

2-66. Vertical Sweep Circuit

The vertical sweep circuit shown in figure FO-2 is discussed functionally on a block diagram level **in** paragraphs 2-28 through 2-31. Paragraphs 2-67 through 2-72 describe the detail functions of **the** stages in this circuitry.

2-67. Sweep Generation **(fig. FO-24)**

Vertical sweep generator **2A4AlAR6 is gated on by a** positive sweep gate from the video simulator and synchronizing circuit. When gated, it produces an output ramp signal that is supplied to summing amplifier **AlAR8**

a. Sweep Generator *Switches 2A4A1Q9, Q10.* These switches operate in the same manner as the horizontal sweep generator switches AlQ3, Q4 (para 2-62a). However, they control application of the sine 0 signal to vertical **sweep** generator AlAR6 instead of the cosine 0 signal.

b. Sweep Generator 2A4A1AR6. This sweep generator stage is electrically identical with horizontal sweep generator A1AR2 (para 2-62*b*). The output from sweep generator A1AR6 is supplied to summing amplifier A1AR8 where it is combined with a vertical offset voltage.

c. Summing Amplifier 2A4A1AR8. Summing amplifier A1AR8 is a hybrid module operational amplifier that combines an offset signal with the output from sweep generator A1AR6. This offset signal is supplied to the summing amplifier through switch A1Q upon application of a yoke clamp signal. The switch is a p-channel fet. ANTENNA switch 2S9 determines the magnitude of the vertical offset signal. With a negative offset voltage applied to the noninverting input of summing amplifier A1AR6, the summing amplifier provides a negative offset output voltage having a magnitude that is three times greater than the offset input. When sweep generator A1AR6 develops a negative ramp voltage, the summing amplifier inverts and multiplies this signal by two; its output is an offset positive ramp voltage.

d. Summing Amplifier Offset Circuit. When the sine θ output is negative, LEFT antenna operation (ANTENNA switch 2S9) with right aircraft drift (NAV SIM control) or right antenna operation with left aircraft drift, the switch 2A4AlQ7 conducts and supplies a zero volt level to source follower AlAR3. The source follower clamps one input to summing network AlR4, R21 at zero volt. Since the other summing network input is a preset voltage between -9.4 and -11.2 vdc, the offset voltage supplied to switch AlQ6 is a dc level between -1.35 and -1.62 volt. When the sine 0 output is positive (right antenna operation with right aircraft drift or left antenna operation with left aircraft drift), polarity sensor driver AlARl provides a high negative voltage that turns switch AlQ8 on and switch AlQ7 off. With switch A1Q8 on, the positive sine 0 output is summed with the fixed vertical offset voltage and routed to switch AlQ6. Setting ANTENNA switch 2S9 to BOTH cuts off switch AlQ7 and permits the polarity sensor driver to control operation of switch AlQ8. Since the polarity of the sine 0 signal alternates in the both antenna mode, switch A1Q8 conducts when the sine 0 signal is positive, charging filter capacitor AlC8. During the other half cycle of the antenna gate, capacitor AlC8 holds its charge to maintain the sine 0 level at the input to summing network AlR4, R21.

2-68. Negative Sweep Detector 2A4A2AR2 and Unipolarizer A2AR4 (fig. FO-24)

Negative sweep detector A2AR2 and unipolarizer A2AR4 operate together to develop negative-going ramp voltages regardless of the polarity of the offset ramp voltage from summing amplifier A1AR8. Output signals from the unipolarizer are supplied to logarithmic amplifier A2AR5 and the dynamic focus circuit. The operation of this circuit is identical with the negative sweep detector and unipolarizer in the horizontal sweep circuit (para 2-64). However, an additional output is taken from negative sweep detector A2AR2. For this output the negative sweep detector acts as an inverter having a gain of one.

2-69. Logarithmic Amplifier 2A4A2AR5 and A2AR7 (fig. FO-24 and 2-14)

Two logarithmic amplifiers are used to modify the horizontal and vertical unipolarized ramp voltages as part of an arithmetic process that provides pincushion corrected vertical deflection signals. Both amplifier circuits are shown in figure 2-14 along with their input and output waveforms. In this illustration, resistors R_a and R_b replace series resistors A2R20, R21 and A2R45, R46 respectively. While the vertical input ramp voltage is between zero and -0.57 volt, the output from logarithmic amplifier A2AR5 increases linearly to +3.4 volts. When the threshold voltage of diode A2CR9 is exceeded, resistor A2R23 is connected in parallel with resistor A2R24 which results in reduced amplifier gain. Thus, as the negative input ramp signal continues to increase, the output waveform shown at B, figure 2-14 is produced This signal approximates the logarithm (to the base 1.6) of ten times the vertical input ramp voltage (waveform A, fig. 2-14). Logarithmic amplifier A2AR7 operates in the same manner as logarithmic amplifier A2AR5. However, since its two break points are at different levels, it provides an output voltage wave shape that follows the logarithm (to the base of 1.6) of the horizontal input ramp voltage squared. These two signals are supplied to threshold summing amplifier A2AR8 through summing network A2R29, R35.

2-70. Threshold Summing Amplifier 2A4A2AR8 and Antilogarithm Amplifier A2AR10 (fig. FO-24 and 2-15)

Threshold summing amplifier A2AR8 and antilogarithm amplifier A2AR10 complete the arithmetic process used to develop vertical pincushion corrected deflection signals. These amplifiers and their input and output waveforms are shown in figure 2-15. The summing amplifier is similar in operation to negative sweep detector A1AR5 in that when its summed inputs (waveforms A and B, fig. 2-15) are below the threshold level of the amplifier, its output is zero volt. As the combined input exceeds this threshold level, the amplifier develops a negative-going signal (waveform C, fig. 2-15). This signal is supplied to antilogarithm amplifier A2AR10. Althouth the antilogarithm amplifier appears similar

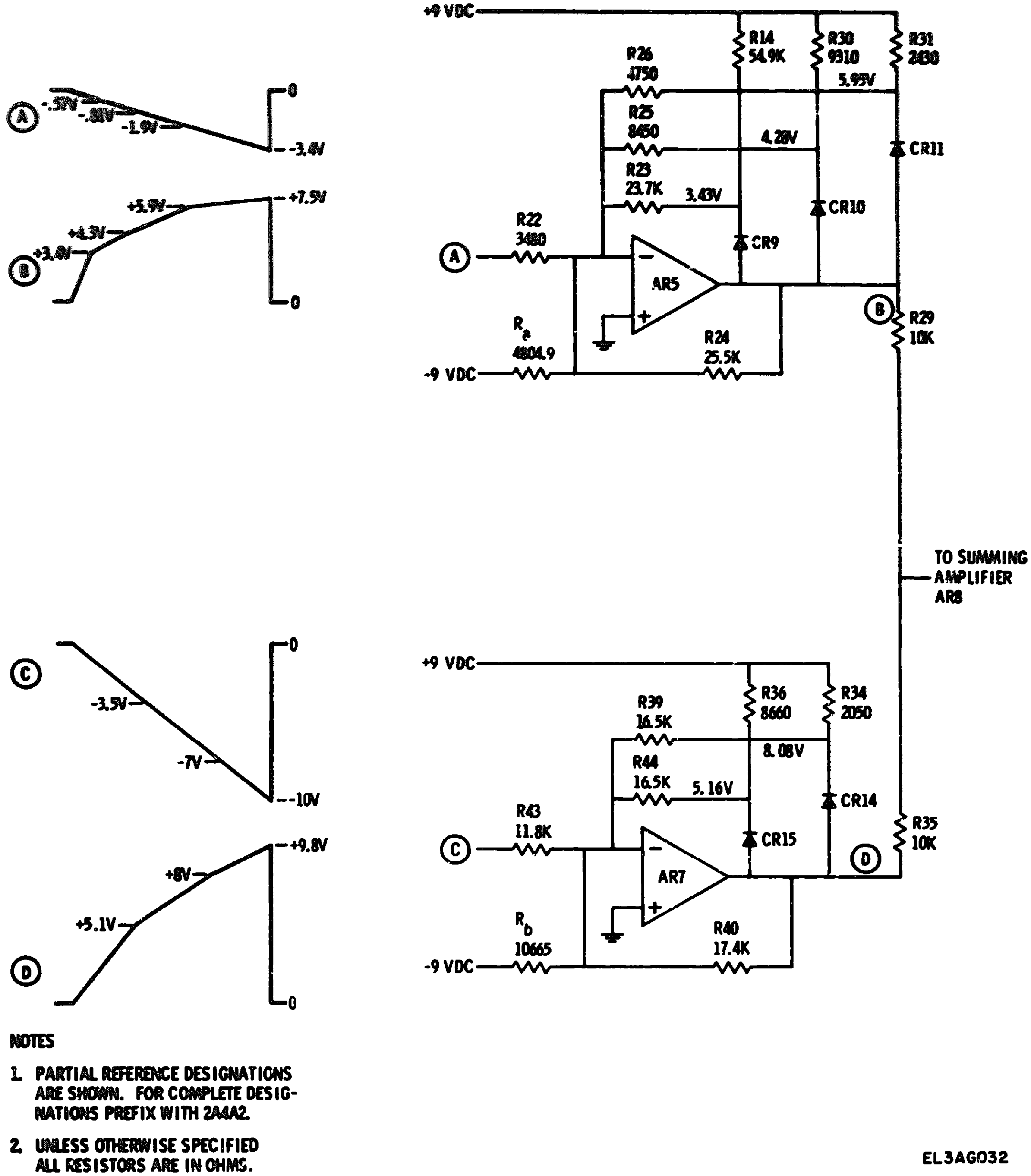


Figure 2-14. Logarithmic amplifiers, simplified schematic diagram.

to logarithm amplifier A2AR5, its operation is somewhat different. With a zero volt level applied to the antilogarithm amplifier input, diodes A2DR18, CR19, and CR20 conduct to parallel resistors A2R64, R57, and R56 with feedback resistor A2R65. As the negative input signal increases (waveform C, fig. 2–15), the inverted output voltage (waveform D) reverse biases diode A2CR19 to increase the gain of the amplifier. This action continues until all three diodes are reverse biased, resulting in an output

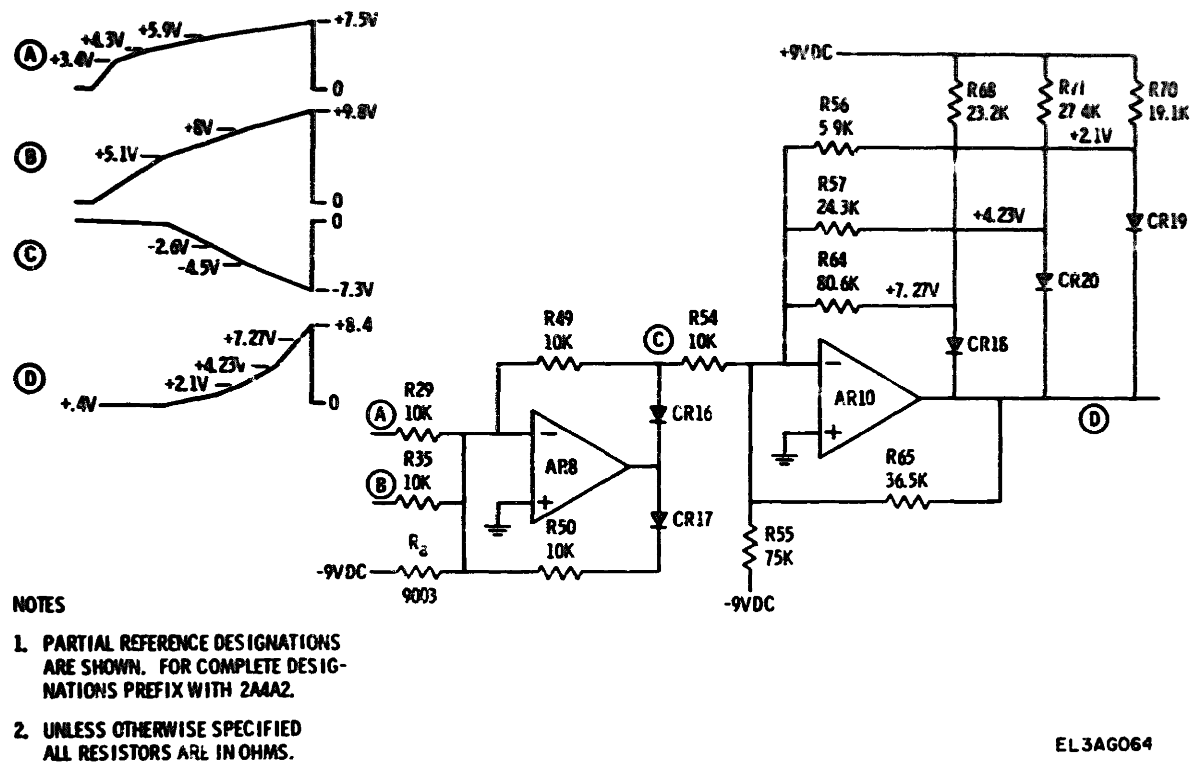


Figure 2-15. Antilogarithmic amplifier circuit, simplified schematic diagram.

voltage wave shape that approximates the antilogarithm (to the base 1.6) of the amplifier input squared +10 volts, divided by 400.

2-71. Vertical Output Switching

(fig. FO-24)

Summing amplifier 2A4A2AR11 combines a sample of the output from antilogarithm amplifier A2AR10 with the offset vertical ramp voltages from summing amplifier A2AR8. Since the ramp voltage can be bipolar and the antilogarithm signal is unipolar, the antilogarithm output is inverted by unity gain inverter A2ARl3 in order to provide complementary antilogarithm signals. The switches A2Ql and Q2 develop complementary samples of the antilogarithm signals across two voltage dividers A2R62/R63 and A2R75/R76. The antilogarithm sample supplied to summing amplifier A2ARll is determined by the operating switch. Control for these switches is provided by limiting amplifier driver A2AR6, which receives the inverted output from negative sweep detector A2AR2 (para 2-63). The limiting amplifier driver acts as an open loop operational amplifier when its output is between ±9 volts. Diodes A2VR2 and CR12 or A2VR3 and CR13 clamp the output voltage at one of these values. Thus, bipolar pulses are produced by the bipolar vertical ramp input signal. These **pulses** are **used** to turn on switches A2Ql and Q2. When the uncorrected vertical sweep signal, from summing amplifier AlAR8, is negative, fet A2Ql is turned on by the negative pulse from limiting amplifier driver A2AR6. This results in the summing of negative vertical ramp voltages with positive antilogarithm sample voltages, by summing amplifier A2ARll. Alternately, positive vertical ramp voltages result in the turn on of switch A2Q2 and the summing of inverted antilogarithm samples with the ramp voltage. This vertical sweep signal is routed to dc amplifier 2A3.

2-72. Direct Current Amplifier 2A3

(fig. FO-23)

The dc amplifier used to supply vertical yoke current for the ft and mt cathode ray tube deflection yokes is identical to the horizontal dc amplifier described in paragraph 2-65.

Section V. VIDEO AMPLIFIER CIRCUIT, CIRCUIT ANALYSIS

2-73. General

The video amplifier circuits are shown in figure FO–2 and discussed functionally, on a block diagram level, in paragraphs 2–32 through 2–36. Paragraphs 2–74 and 2–75 describe the detail functions of the stages in this circuitry. The circuits discussed are fixed-target video amplifier 1A2A6 and cathode ray tube unblanking.

2-74. Fixed-Target Video Amplifier 1A2A6 (fig. FO-20)

Video amplifier 1A2A6 contains circuitry for controlling blanking and unblanking of the ft cathode ray tube as well as a video amplifier circuit. In the video amplifier, positive fixed target or test video signals, from relay 1A2K4 (fig. FO–2), are ac coupled to complementary input amplifier A2Q2, Q3. Potentiometer A2R2 is adjusted for a 2-volt peak video input signal minimum. Dc voltages for the amplifier are derived from the module plus and minus 20 vdc inputs. Zener diode regulator A2VR1 develops -15 vdc from the -20-volt source while the +20-volt input is decoupled and supplied direct to the input amplifier. The amplifier increases the signal amplitude to approximately 12-volts peak without introducing phase inversion and ac couples its output to temperature stabilized emitter *follower* A2Q4. Since the de reference is lost due to ac coupling, dc restorer A2CR1, CR2, R9 is used to clamp the signal base line at zero vdc. In the dc restorer, diode A2CRl compensates for the voltage drop across diode A2CR2. The output from emitter follower A2Q4 is applied to a fixed compression network consisting of resistors A2Rl2/R13, and temperature stabilized diode A2CR3. When the amplitude of the signal is below the diode threshold, the signal is coupled through capacitor A2C8 to complementary amplifier A2Q5/Q6. As the amplitude of the signal increases above the diode threshold, the signal supplied to amplifier Q2Q5/Q6 is divided by voltage divider A2R12/Rl3. This effectively decreases the overall gain of the video amplifier for large signal inputs. The second complementary amplifier (Q5/Q6) and emitter follower A2Q7 are identical with the input amplifier circuit. Dc restorer A2CR4, CR5 and R20 is used to clamp the base line of the video input signal at zero vdc in the same manner as dc restorer A2CR1, CR2, R9. Output signals from emitter follower A2Q7 are supplied to output emitter follower A2Q8. Three selectable compression networks A2CR7/R26, CR8/R27, and CR9/R28 introduce additional compression depending upon the settings of ANTENNA switch 2S9 and RANGE switch 2S8 (para 2–32). These diodes are either reverse biased by +15 vdc or returned to ground. The output from emitter follower A2Q8 is routed to FT GAIN potentiometer 1A2R6 (fig. FO–2) and returned through pin U to diode clamp A1CR11. This diode clamps the video signal base line at a level determined by INTENSITY potentiometer 2R6 in parallel with resistors 2A1R25 and R26 (fig. FO–22).

2-75. Cathode Ray Tube Unblanking (fig. FO–20)

Unblanking of the fixed-target cathode ray tube is controlled by transistor switch 1A2A6A1Q10. When the switch conducts, the cathode of the crt is clamped at a +31 vdc level established by Zener diode A1VR3. With switch A1Q10 cut off, the crt cathode voltage rises to +100 vdc and cuts off the cathode ray tube. Reverse bias for switch A1Q10 is provided by diode A1CR17 and resistor A1R42. Diode A1CR16 protects the cathode ray tube from damage in the event of a +100 vdc source failure. Transistor A1Q10 is switched on and off by the output of diode AND gate A1CR12, CR13, CR14, CR18. This gate receives two direct inputs from the video simulator and synchronizing circuit and one from UNBLANK switch 1A2S6 (fig. FO–2). The fourth input is derived from the yoke feedback signal in the fixed target horizontal sweep circuit. This signal is a bipolar sweep signal that is coupled to unipolarizer A1AR1 through capacitors A1C21, C22. The unipolarizer is a variable gain operational amplifier that provides a negative gate for each sweep signal input. Zener diode A1VR6 reduces the gain of the amplifier when the feedback voltage appearing across resistor A1R38 exceeds 4.3 volts. Positive input signals passing through diode A1CR19 are inverted by A1AR1 while negative inputs that pass through diode A1CR20 develop output gates without inversion. The negative gates are translated through diodes A1CR21, CR22, and CR23 to turn compound-connected switch A1Q9 off. At the end of the gate signal, capacitor A1C20 charges through resistor A1R39 to hold the transistor switch off until the next gate signal occurs. If the horizontal sweep signal is lost, switch A1Q9 conducts, turning off switch A1Q10. Switch A1Q12 suppresses transients when UNBLANK switch 1A2S6 (fig. FO–2) is operated to protect the cathode ray tube.

Section VI. CATHODE RAY TUBE FOCUS CIRCUIT, CIRCUIT ANALYSIS

2-76. General

The cathode ray tube focus circuits are shown on figure FO-2 and discussed functionally, on a block diagram level, in paragraphs 2-34 through 2-36. Paragraphs 2-77 through 2-81 describe the detail functions of the stages in this circuitry. Circuits discussed are as follows: ft and mt dynamic focus circuit, squaring amplifier 2A4AAR9, dynamic focus amplifier, drift angle servo loop, servoamplifier, and servo loop stepper motor.

2-77. Ft. and Mt Dynamic Focus Circuit (fig. FO-24)

Both the ft and mt dynamic focus amplifiers receive their signal input from squaring amplifier 2A4AlAR9. Since the amplifiers are identical, only the ft dynamic focus amplifier is described. Paragraph 2-78 discusses operation of the squaring amplifier.

2-78. Squaring Amplifier 2A4A1AR9 (fig. 2-16)

The squaring amplifier modifies unipolarized horizontal and vertical ramp voltages to provide the proper wave shape for dynamic focusing of the cathode ray tube electron beams. The amplifier and its input and output waveforms are shown in figure 2-16. In this illustration, resistor R_a replaces series resistors A1R47 and R48 (fig. FO-24). When the unipolarized horizontal ramp signal (waveform A) is between 0 and -0.7 volt, diodes A1CR7, CR8 and CR9 are reverse baised. Diode A1CR6 is cut off also, since the unipolarized vertical ramp signal (waveform B) is less than -0.7 volt during this interval. Under these conditions the squaring amplifier input is balanced to ground causing its output to be zero volt. The input network is unbalanced when the threshold level for diode A1CR7 is exceeded. This causes the junction of resistors AlR40, R44 to track the input signal down to its maximum value, producing a positive going amplifier output. Exceeding the threshold levels of diodes AlCR8 and CR9 causes the junctions of resistors AlR41, R45, and AlR42, R46 to track the input signal also. Thus, the gain of amplifier AlAR9 is increased at each break point. For the horizontal and vertical ramp signal amplitudes shown in figure 2-16, the threshold for diode AlCR is exceeded when the horizontal ramp input is approximately -2 volts. Beyond this point the horizontal and vertical signals are added at the input of the squaring amplifier. The output from the squaring amplifier (waveform C) approximates the sum of the squares of the input ramp signals divided by 11.47.

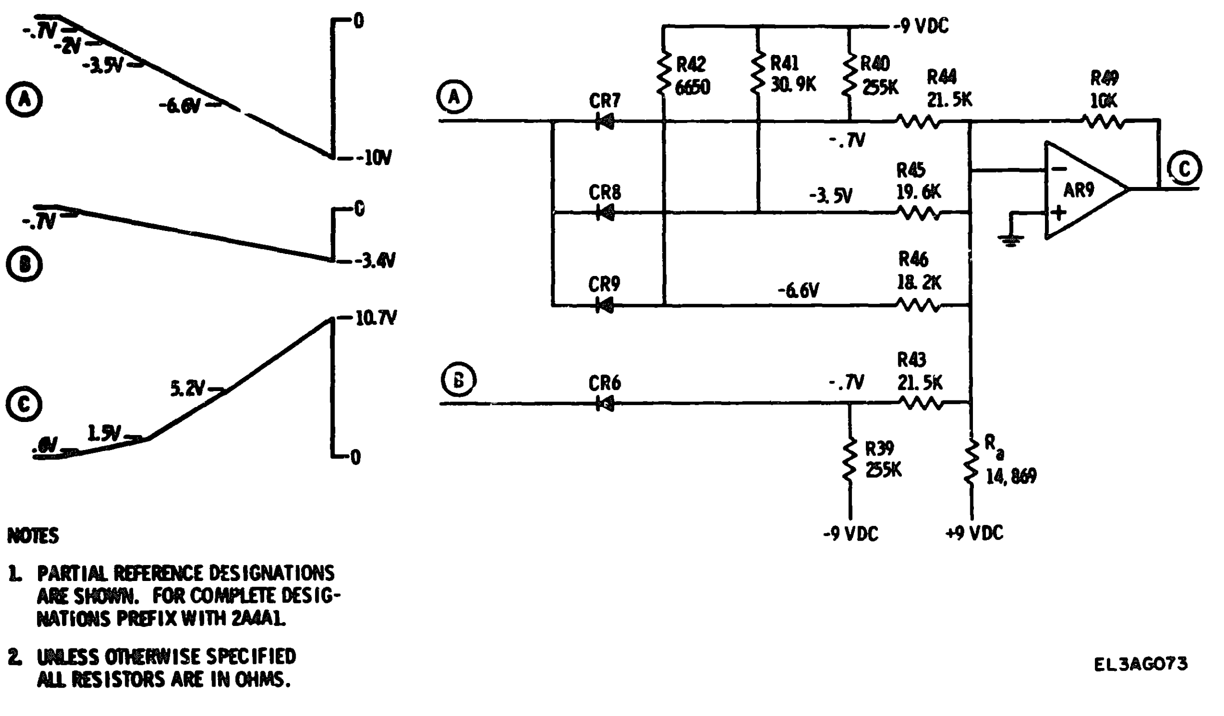


Figure 2-16. Squaring amplifier circuit, simplified schematic diagram

2-79. Drift Angle Servo Loop (fig. FO-3)

The drift angle servo loop consists essentially of the NAV SIM control mechanical linkage, synchro transmitter 2B2, synchro receiver 1A2B1, servoamplifier 2A5, and stepper motor 2B1 (fig. FO–3). GS/DFT DRIVE switch 2S12 (fig. FO–3) supplies +20 vdc to the servo amplifier drivers in the ON position. If NAVIGATION Switch 2S6 (fig. FO–3) is set to AUTO, and relay 2A5A2K1 (fig. FO–3) operates, ±20 vdc is supplied to the drift angle and groundspeed servoamplifiers. With SERVO LOOP switch 2S7 set to DFT, the rotor and stator windings of receiver 1A2B1 are connected to the servoamplifier and transmitter 2B2 through relays 1A2K5 and K6.

2-80. Servoamplifer (fig. FO-25 and FO-3)

Servo amplifier 2A5 contains two indentical amplifiers. One is used in the drift angle servo loop and the other is used in the groundspeed servo loop. Since the amplifiers are identical, only stages of the drift angle servoamplifier are discussed.

a. Buffer A3AR. On alternate half cycles of a 26-vac, 400-Hz reference signal from transformer lA2Tl (fig. FO–14), switch A3Q5 (fig. FO-25) conducts through amplifier A3Q6 and switches A3Q7, Q8 to drive buffer A3AR5. During the other half cycle when the switch is cut off, a sample of the 49-Hz drift angle information is supplied to the inverting input of buffer A3AR5. The buffer is a micromodule operational amplifier having a voltage gain of approximately 45, which is established by feedback voltage divider A3AR9, R37. Waveform B (fig. FO-3), represents the buffered output signal when the error signal between synchros lA3Bl and 2B2 is less than 5 degrees. For an error of greater than 5 degrees, the buffer is overdriven which produces a square wave output signal.

b. Integrator *A3AR6.* Integrator A3AR6 is a bootstrap generator that develops positive or negative ramp output signals depending upon the polarity of the output from buffer A3AR5. Since the ramp generator input is a pulsating dc signal, charging capacitor A3C17 holds its output charge during the intervals when the rectifier output is clamped to ground, causing integration of the output from buffer A3AR5. Adjustable degenerative feedback is provided by voltage divider A3R48/R49, and R50 to permit adjustment of the ramp generator voltage gain for *a* value of 2. Charging resistor A3R40 and bootstrap resistor R47 operate together to establish a constant charging current through capacitor A3Cl7. With a constant current flowing through the capacitor, a linear ramp voltage is developed at the output of integrator A3AR6 (waveform C, fig. FO-3).

c. Level Detectors A3AR7, AR8. Level detectors A3AR7, AR8 are micromodule operational amplifiers incorporating external positive feedback. Positive and negative 1.14 vdc bias voltage is developed from two voltage dividers, A3R51/R52 and A3R53/R54. The positive bias is supplied to the noninverting input of level detector A3AR7, while the negative bias is applied to the inverting input of level detector AR8. Ramp voltages from integrator A3AR6 are fed to the remaining input of both level detectors. When the peak of the ramp voltage is less than the 1.5 volt threshold of the level detectors, the output from both detectors is approximately +7 vdc. If a positive ramp exceeds the threshold of level detector A3AR7, its output switches, producing a negative transient that turns on transistor switches A3Q11, Q10 and Q9 through monostable multivibrator A2U8A, U12B and inverter A2U7C. With transistor switches Q9, Q10 on, charging capacitor A3C17 discharges, causing the output of level detector A3AR7 to return to +7 vdc (waveform D, fig. FO–3). The monostable stretches the output pulse of detector A3AR7 to provide sufficient time for discharge of the capacitor. If a negative ramp voltage from integrator A3R6 exceeds the threshold of level detector A3AR8, its output also goes low, turning on switches A3Q11, Q9, and Q10 in a similar manner.

d. Stepper Motor Control Circuit. The stepper motor control circuit consists of two digital comparators consisting of micromodules A2U110A, A2U9D, A2U10B, A2U9C and two bistable multivibrators A2U11A and UllB. The negative-going pulse from a level detector is transformed by level changer U9A, U9B into complementary inputs at comparators A2U10A, U10B. Each comparator performs an AND-OR-INVERT logic function for the complementary inputs and the crosscoupled outputs from bistable multivibrators A2U11A, U11B to provide the clock steering gates for the J-K inputs. The clock pulse is coupled through monostable multivibrator A2U8A, U12B and delay inverter A2U12A, U12C, U12D to the bistable trigger inputs. The time constant of A2C14, RN, plus the inherent time delays of A2U8A, U12B, U12A, U12C and U12D provide time for the J-K inputs to stabilize before the clock pulse arrives. When triggered, the bistables provide an enable gate for inverters A2U7A, U7E or U7D, U7F, depending on which level detector is providing an output. Simultaneously with the application of the bistable steering gates, the level detector pulse is inverted by A2U8B and applied to inverter A2U7B. Switch A2Q13 and emitter follower A2Q14 provide a delayed output pulse for each input pulse. Before the switch can turn on, capacitor A2C8 must discharge through resistor A2R25. When the input pulse is removed, A2C8 must charge to the A2Q14 cutoff level through resistors A2R26 and R22. The collector out of

A2Q13 is commonly connected to the driver inputs through load resistors A2R29, R31, R33, and R35. The output pulse, therefore, will forward bias the two driver inputs that are enabled by the logic circuitry. The forward-biased driver pair then conducts current through the logically selected motor windings (fig. FO–3).

2-81. Servo Loop Stepper Motor (fig. 2-17)

Internal construction of the stepper motor is represented in view B, figure 2–17. As shown in view B, two coils are wound on each stator pole. These windings are connected to produce polarization of the stator poles as indicated at view A. Assuming that switches 2A5A2Q18 and Q16 are forward biased, all A and B coils are energized causing stators 1, 2, 5, and 6 to become south poles and stators 3, 4, 7, and 8 to become north poles. Since the permanent magnet rotor tends to position itself to balance all magnetic fields, the rotor assumes the position shown in view B. If transistors 2A5A2Q17 and Q15 are forward biased, the A and B windings are energized providing the polarization indicated in view A. Sequencing of the switches is determined by the stepper motor control circuit. Waveforms J through L of (fig. FO–3) illustrate switch sequencing as the error signal passes through a null.

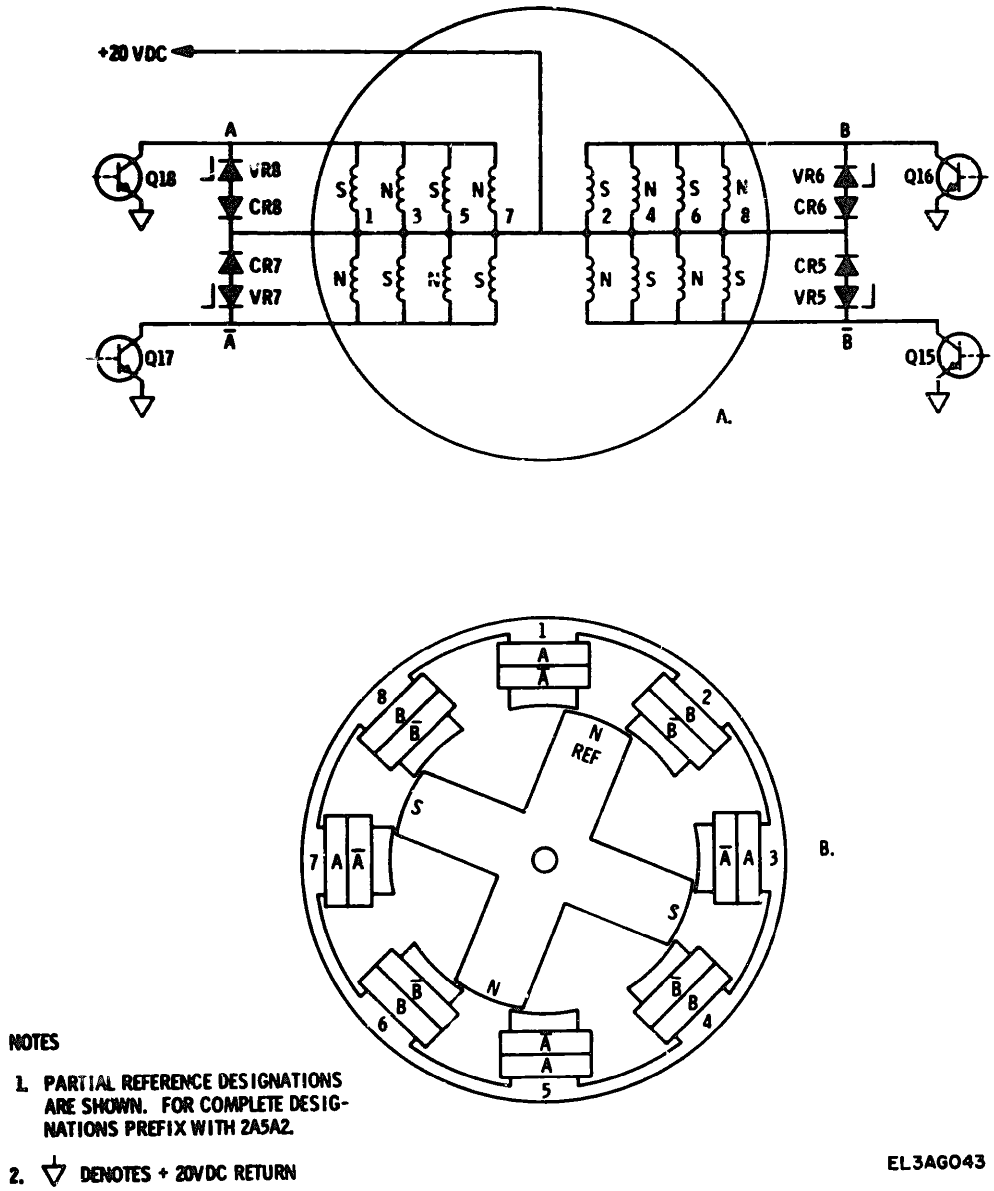


Figure 2-17. Stepper motor contol, simplified schematic diagram

Section VII. BITE AND POWER SUPPLY CIRCUITS, CIRCUIT ANALYSIS

2-82. General

The BITE circuits are shown in figure 2-8 and discussed functionally, on a block diagram level, in paragraph 2-42. Paragraph 2-83 describes the detail functions of the stages in this circuitry. The power supply circuits are shown on figures 2-4 through 2-6 and discussed functionally, on a block diagram level, in paragraphs 2-38 through 2-40. Paragraphs 2-84 through 2-92 describe the detail functions of the stages in this circuitry. Circuits discussed are as follows: indicating system series regulated supplies, indicating system shunt regulated supplies, indicating system overcurrent protection, secondary power sources, low voltage power supplies, anode and focus loads, and film speed variable voltage source.

2-83. BITE Circuitry (fig. FO-18)

The BITE circuitry is divided into two major circuits which are functionally described on a block diagram level in paragraph 2-42. Detailed stage analysis of both major circuits are discussed in a and b below.

a. Primary Fault Detection Circuit. The primary fault detection circuit causes FAILURE lamp lA2DS2 (fig. FO-14) to light if an overvoltage or undervoltage condition exists for the horizontal sweep, vertical sweep, video, or unblank signal. Outputs of the four sensing circuits are commonly connected to the base of switch lA2A4Ql so that a positive output from any channel will turn on the switch to provide a circuit path through the FAILURE lamp. Also, voltage clamps in comparators lA2A4AR2, AR4, AR6, and AR8 are commonly connected through BITE switch lA2S7 (fig. FO-14) to ground in the OFF position. When BITE switch lA2S7 is placed in the ON position, the four sensing circuits are enabled. Since circuitry is essentially the same for all four channels, only the video fault detection channel is discussed. A sample of the ft video signal is applied to operational amplifier lA2A4AR5 which has a gain of approximately 0.5 Diodes CR5, CR6, and CR14 provide voltage limiting. The amplifier positive output is peak detected by CR7 and C35. This dc level appears at pins 4 and 7 of dual comparator AR6. Pin 6 of one comparator is referenced to +l vdc, and pin 3 of the other comparator is referenced to +10 vdc. If the video signal rises above the +10 volt reference, a noninverted (positive) output occurs. If the signal drops below +1 volt, a positive output also occurs. In either failure mode, switch Ql is turned on.

b. Fault Isolation Circuit. The fault isolation circuit contains two circuits: a high voltage power supply monitor circuit and a servo fault circuit When connected to Recorder-Processor-Viewer, Radar Mapping RO-495/U, a BITE signal from the high voltage power supply enables switch 2A1Q8 to allow INDICATOR FAULT lamp DS2 to flash (para 2-44). The servo fault circuit in the fault isolation circuit (fig. 2-8) consists of two integrating amplifiers. 2A5A1Q6 and Q7, two emitter followers Q2 and Q3, threshold switch Q4, switch Q5, and switch 2A1Q7. Transistors Q6 and Q2 perform the same functions for the groundspeed servo as transistors Q7 and Q3 do for the drift angle servo. As the drift angle servo error increases, the pulse train pulse repetition frequency from gate 2A5A2U7C increases, causing capacitor 2A5A1C6 to hold its charge throughout the interpulse period. Thus, the average positive dc level at the output of emitter follower Q3 increases until the 5-volt threshold level at the base of threshold switch Q4 is exceeded. When the threshold is exceeded, switches 2A5A1Q4 and Q5 turn off, and allow a stable multivibrator 2A7A2Q1, Q2 (fig. FO-27) to control the operation of the SERVO FAULT indicator through switch 2A1Q7.

2-84. Indicating System Series Regulated Supplies (fig. FO-12)

a. General. Transformer Tl in low voltage power supply module lAlA3 develops six three-phase voltages from the 115 vac, 400 Hz primary power. These voltages are rectified by six three-phase bridge rectifiers. The unregulated outputs from these rectifiers are routed to five series-regulator and a shunt-regulator circuit.

b. Regulated -28-Volt DC Supply. Series regulator lAlA3Ql supplies regulated -28 vdc to the other regulator circuits. If the -28 vdc supply does not provide its normal output, the remaining supplies are disabled. A sample (referenced to ground) of the regulated -28 vdc is taken from potentiometer A4AlR13 (fig. FO-12) and supplied to differential amplifier A4AlQ3 where it is compared with a signal (normally 16.3 volts dc) developed by 11.7-volt Zener diode A4AlVR2. Any change in the regulated output voltage is divided by voltage divider A4AlR12, R13, R14. Thus, an increase in the -28-volt output (more negative) causes the differential amplifier to produce a positive-going error voltage for inverter A4AlQ2. Because the inverter supplies base current for series regulator lAlA3Q1, its collector current decreases, causing the regulated output voltage to return to its original value. Zener diode A4AlVRl assures proper starting of the regulator. When primary power is applied, the regulator output is zero volt. Base current for series regulator lAlA3Ql (fig. FO-12) is supplied through diode A4AlCR3 and 27-volt Zener diode A4A1VR1. As the regulator output rises toward the -37-volt unregulated voltage, differential amplifier A4A1Q3 and inverter A4A1Q2 become active, to reverse bias diode A4A1CR3, and disable the starting circuit.

c. Regulated -20-Volt Dc Supply. Series regulator 1A1A3Q4 (fig. FO-12) operates in a circuit that is similar to the -28 vdc regulator circuit. However, differential amplifier A4A2Q1 receives its supply voltage reference voltage from the *regulated* -28 vdc output. A -20 vdc reference voltage, developed by voltage divider A4A2R5 through R8, is *compared* with the -20-volt supply regulated output in differential amplifier A4A2Ql. Any change in this output is inverted by the differential amplifier and supplied to inverter lAlA3Q5 where it is again inverted. The output from inverter Q5 is used to provide drive for series regulator lAlA3Q4. Since the series regulator also acts as an inverter, any change in output voltage is canceled. Output filtering is incorporated by parallel capacitors 2C4, C5, C6 (fig. FO-21).

d. Regulated +100-, +20-, and +6 3-Volt Dc Supplies. The +100-volt, +20-volt, and +6.3-volt series regulators lAlA3Q7, Q2, and Q6 are driven by similar regulator circuits. In each case, differential amplifiers A4A2Q2/Q3; A4AlQl; and A4A1Q5, respectively (fig. FO-12) receive input voltage from the regulated output of the -28 vdc supply. Voltage dividers between the respective regulated output and the regulated -28 volts provide a zero volt signal to the differential amplifiers. These signals are compared with a ground reference in the differential amplifiers to develop error output signals. In the +100-volt regulator, the error signal is routed directly to series regulator 1AlA3Q7 while error signals for the +20- and +6.3-volt supplies are routed through emitter follower lAlA3Q3 and inverter A4AlQ4 respectively, before being applied to their series regulators. Output filtering, for the +20 vdc power supply, is provided by capacitors 2C1, C2, C3 (fig. FO-21). Back-to-back diodes A4A2CR3, CR4 and A4AlCR1, CR2 limit excursion of the input error signal to ±0.7 volt, for the +100- and +20-volt regulators, to prevent damage to their differential amplifiers.

2-85. Indicating System Shunt Regulated Supplies
(fig. FO-12)

A shunt regulator is fed by the 665-volt unregulated output of three-phase rectifier lAlA3AlCR13 through CR18. The regulator (lAlA3Q8) provides 531 **volts** dc. This regulator is controlled by emitter follower A4A2Q4 which receives a sample of the regulated output from voltage divider A4A2R22, R23, R24, CR6, CR7. The emitter follower receives its source voltage from the regulated +2-volt supply and references the sample signal to the -28 vdc output voltage.

2-86. Indicating System Overcurrent Protection
(fig. FO- 12)

Silicon controlled rectifier switch A3AlQl operates relay A3AlK3 in the event that either the plus or minus 20-volt supply is overloaded. With relay A3AlK3 **operated, series regulator lAlA3Ql** is cut off which removes the -28 vdc power thereby turning off **the** other series regulators. Switch A3A1VR1 conducts when it receives a positive pulse **at** its gate and remains on until its anode **voltage** is removed. Normally, a negative voltage is supplied **to the switch** through resistor A3AlR2. If either current relay A3AlKl or K2 operate, unregulated +20 vdc is connected to voltage divider A3A1Rl/R2 This generates a positive pulse that exceeds the threshold voltage of 12-volt Zener diode A3A1VRl to trigger the silicon controlled rectifier resulting in the turn off of all six power supplies.

2-87. Secondary Power Sources
(fig. FO-26 and FO-8)

a. Fifteen-Volt Regulators. Plus and minus 15 volts are developed from the regulated ±20-volt sources by two series regulator circuits. Operation of the +15-volt regulator is the same as for the +20-volt supply discussed in paragraph 2-84. Two provide negative voltage, a -15-volt reference voltage is derived from the regulated -28 vdc power supply by voltage divider 2A6AlR16, R17 (fig. FO-26). This dc level is compared with the output -l&volt regulator by noninverting differential amplifier 2A6A1Q2. Output from the differential amplifier is direct coupled through emitter follower 2A6AlQl to provide base current for series regulator 2Q2 (fig. FO-8). Since the series regulator acts as an inverter, variations in the nominal -15 vdc output level are canceled.

b. Secondary Power Source Overcurrent Protection. Switch 2A6Ql and switch 2A6Q2 (fig. FO-26) provide overcurrent protection in the +15-volt dc and -15-volt dc regulator circuits. Both overcurrent protection circuits function in a similar manner; consequently, only the +15-volt dc overcurrent protection circuit is discussed. Any time that the output of the +15-volt dc regulator falls below approximately 13 volts dc, Zener diode 2A6VRl conducts, causing switch 2A6Ql to turn on. With switch 2R6Ql turned on, the base of emitter follower 2A6AlQ3 is clamped to the +20-volt dc regulated output, which turns off this stage, thereby removing the base current from series regulator 2Ql (fig. FO-6).

c. *Nine-Volt Sources.* Plus and minus 9 vdc is generated by cascade operational amplifiers in module 2A4. One amplifier (2A4A2ARl) (fig. FO-24) is connected as a source follower and is used to provide a low impedance source having power gain. This amplifier receives +9 volts at its noninverting input. This voltage is derived from the +15-volt dc regulator through 11.7-volt Zener diode 2A4A2VR1 and potentiometer 2A4A2R2. The output of 2A4A2AR1 is used by circuitry within the sweep generator. This output is fed also to operational amplifier 2A4A2AR3 which is connected as an inverting amplifier having a gain of one; thus, its output is -9 vdc. This voltage is used by the circuits in the sweep generator also.

d. Groundspeed/Drift Ang . Servo Sources. Four secondary voltages are supplied by regulators in module 2A5 (fig. FO—25). Two of the regulators (2A5A3Q12 and 2A5A1Q1) are conventional series regulators using Zener diodes as their references. Regulator 2A5A3Q12 provides a plus 12-volt source for operational amplifiers 2A5A3AR3, AR4, AR7, and AR8; while regulator 2A5A3Q1 supplies a plus 5-volt level for the digital micromodule circuitry. The remaining two secondary voltages (plus and minus 6 volts) are supplied by transistors 2A5A3Q13, Q14, and Q15. Transistor Q13 is a conventional Zener referenced series regulator that provides the plus 6-volt output. Series regulator Q15 receives its drive signal from inverter Ql4; which, in turn, receives an error signal from the temperature compensated voltage divider across the plus and minus regulated outputs. Thus, the negative voltage tracks the positive voltage to maintain balanced outputs. Zener diode VR3 is normally cutoff, but it is incorporated to prevent the negative output from exceeding 8-volts at turn on or as a result of noise transients.

2-88. Low Voltage Power Supplies (Module

(fig. FO-17)

a. General. Transformer lA2T2 (fig. FO-14) develops three, three-phase voltages from the 115 vac, 400-Hz primary power. These voltages are rectified by three, three-phase bridge rectifiers. The unregulated outputs from these rectifiers are filtered and fed to three series regulated power supplies.

b. Plus 28 *Vdc Supply.* A sample of the output of series regulator lA2A3Q9 (fig. FO-17) is taken from diode temperature-compensated voltage divider CR20, CR19, R29, R28 and applied to error amplifier input stage Q10. The emitter is clamped at 11.7 volts by Zener diode VR4. Any voltage change in the output of series regulator Q9 is inverted and amplified by Q10 and supplied through driver Q8 to the base of Q9. Consequently, an increase or decrease in emitter voltage of Q9 causes a decrease or increase, respectively, in conduction through Q9. Resistor R27 supplies starting current to Q10. Switch Q11 provides short circuit protection. Q7 is a constant current source for Q9. If the emitter voltage of Q9 approaches ground potential, normally-on switch Q11 turns off and Zener diode VR3 ceases to conduct. The base of constant current source Q7 is switched to 33 volts causing this stage to turn off, thereby turning off Q8 and Q9.

c. Plus 20 Vdc Supply. The +20 vdc supply circuit consists primarily of series voltage regulator 1A2A3AR1. This regulator receives input power from the +28 vdc supply at terminal 5 and is case grounded to +28 vdc circuit ground. The regulated output is sampled at the junction of R21, R22 and supplied to terminals 4 and 5. Capacitors C8 and C7 provide filtering. Network R18, R19, R20 establishes the output voltage regulation point. Voltage divider R22/P41 provides startup current. Short circuit shutdown is provided by switch Q13 which turns off in the event of a short circuit to supply a +20 vdc shutdown signal.

d. Minus 5 Vdc Supply. The -5 vdc supply functions in a manner similar to the +20 vdc supply. Unregulated input voltage is supplied to terminal 3 of series voltage regulator 1A2A3AR2. Resistors R42 and R17 supply start up current. Switch Q12 turns off when the -5 vdc output approaches circuit ground and shuts down the series regulator.

e. ***Plus 5 Vdc Supply.*** The +5 vdc supply functions in a manner similar to the +28 vdc supply. However, the regulated output is referenced to the regulated output of the -5 vdc supply through series resistors lA2A3R11, R12. Differential amplifier Q6 senses any relative change in the regulated outputs of the 5 **vdc** supplies, causing driver Q2 and series regulator Q3 to operate to null the change. If the +5 vdc regulated output approaches circuit ground potential, switch Q4 turns off, causing switch Q5 to turn off. With Q5 off, current source Q1 turns off, which causes series regulator Q3 to turn off. Start up current is provided by resistors R4 R13 and Zener diode VR2 which ceases to conduct as output voltage rises.

2-89. Anode and Focus Loads (fig. *FO-9)*

Anode load module lA1A6 and focus load module lAlA5 provide a means of measuring regulated or unregulated anode and focus voltages and the ripple voltage content of these voltages. For the purpose of clarity, only those test set group cable connections ***of*** immediate interest are discussed.

a. *Anode* Load When the anode voltage to be checked is connected to connector lAlJ8, series resistors lAlA6R3-R6 and lAlA2R1 provide a 1000-megohm dc load. The voltage drop across the parallel resistance of lAlA6R6 and lAlA2Rl provides the input to the anode voltage follower lAlA2U1. The output of the voltage follower is monitored at ANODE VOLTAGE 1V/10KV test jack E3. Capacitor Cl decouples the high voltage dc to permit ripple voltage measurements which are taken across resistor 1A1A5R1 via ANODE RIPPLE test jack E1. Neon gas tubes 1A1A6DS1–DS3 limit transient voltages across resistor 1A1R1 to approximately 270 volts. Resistor 1A1A6R2 limits current through the neon gas tubes during periods of conduction. Test jacks 1A1A6E2, E3, and E5 provide test points for checking operation of the neon gas tubes.

b. Focus Load. Focus load module 1A1A5 functions in a manner similar to that covered in *a* above with the following exceptions: Series resistors 1A1A5R3 – R6 and 1A1A2R4 provide a 55-megohm dc load. The voltage drop across the parallel resistance of 1A1A5R6 and 1A1A2R4 provides the input to the focus voltage follower 1A1A2U2. The output of the voltage follower is monitored at FOCUS VOLTAGE 2.75V/2.7kV test jack E4.

2-90. Film Speed Sources

There are two film speed sources. One is used to test the interconnections of unit 5 and the load of unit 9. The other provides calibrated film speed levels along with 115 vac servo for film speed servo.

a. RO–495/U Unit 5, Unit 9 Interconnect Test. The circuit shown in figure 2-18 provides a +4v to +27v dc potential, depending upon the setting of FILM SPEED control 1A2R18. When this control is fully clockwise, maximum voltage is developed by conduction through emitter follower 1A2A4Q4. As the control is rotated in the counterclockwise direction, amplifier Q5 begins to conduct. The emitter of Q4 follows its decreasing base potential until it reaches a level a few tenths of a volt less than the emitter clamp potential of Q5.

b. Calibrated Film Speed Circuit. The calibrated film speed circuit consists of transformer 1A1T1, FILM SPEED switch 1A1S3 and voltage divider 1A1A2R15 – R18. The divider output is approximately 0 to 13.2 vac. These voltages are used to control the film drive servo in Recorder-Processor-Viewer, Radar Mapping RO–495/U during maintenance. This circuit is shown in figure 2–19.

2-91. Regulated +28 Volt Dc Supply and High Voltage Loads

(fig. 2-9)

Plus 28 Vdc regulated voltage is generated from the 196 Vac between phases in the 1A1 panel assembly with transformer 1A1T1, reactor 1A1L1 and the regulator circuit on lAlA2. The primary power is applied to the primary winding of transformer 1A1T1. A 43-volt ac secondary is applied to bridge rectifier 1AlA2CRl - CR4, the output of which is

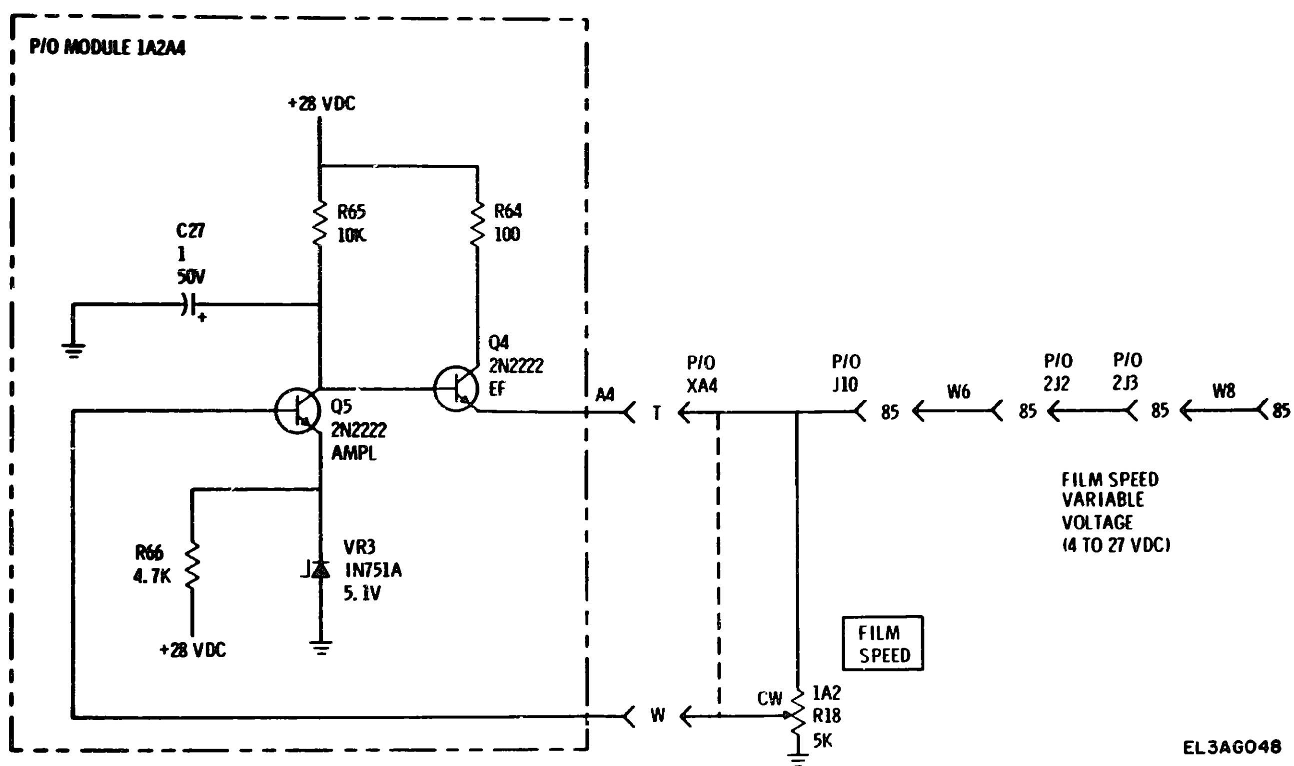


Figure 2-18. film speed variable voltage circuit,, simplified schematic diagram

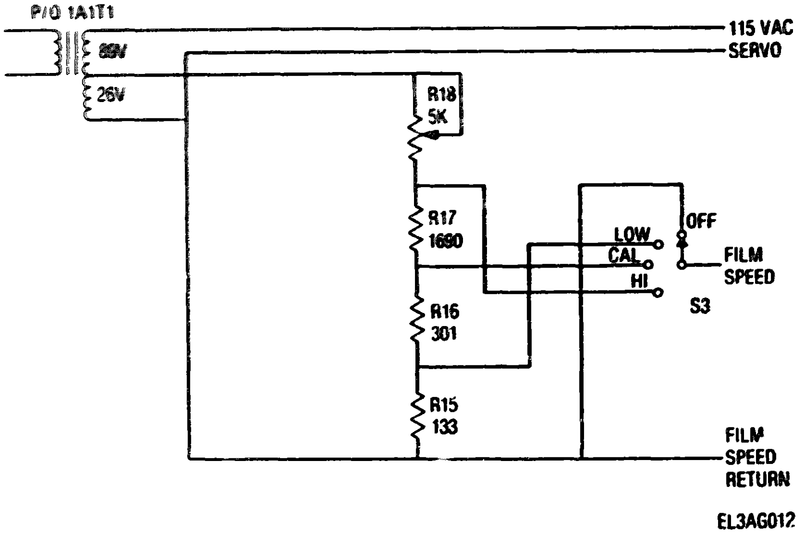


Figure 2-19. Control film speed control circuit

filtered by LC network lAlL1, lAlA2Cl. Power amplifiers lAlA2Q1, Q2 amplify the rectified voltage and feed regulator lAlA2Q3 which develops the output of +28 volts dc. The regulated +28 vdc is used for the film speed servo assembly and the input to VR7 which outputs +5 vdc to the ADAS board.

2-92. Plus 26 Volt DC Power Supply

The +26 Vdc power supply is a dc-to-dc power supply. It is a sealed, non-rep&able module. Its output is used to test the high voltage power supply in the RO-495/U.

Section VIII. ADAS SIMULATOR CIRCUITS, CIRCUIT ANALYSIS

2-93. ADAS Simulator

(fig. FO-10).

ADAS simulator lAlA1 provides unblanking and vertical deflection signals which exercise the ADAS printer circuitry of Recorder-Processor-Viewer, Radar Mapping RO-495/U. The ADAS simulator has three operating modes as set by ADAS MODE switch 1AlSl: BCD, NUM, and ALT. In the BCD mode, BCD ADAS data blocks are generated by the ADAS simulator and output as a series of +80 vdc unblanking pulses. The vertical deflection signal (-20 to +14 vdc ramp) is enabled after each six bits of data in this mode. In the NUM (numeric) data mode, the unblanking pulses are again output, but the ramp signal is disabled. The vertical deflection signal, in this mode, is produced by a deflection clock circuit. In the ALT (alternate) mode, the ADAS simulator switches between BCD and numeric modes for alternate ADAS data blocks. The following subparagraphs describe the circuits of the ADAS simulator.

a Input Buffer and Clock Enable. Input buffer lAlQ1 accepts the 28 volt data demand pulse and converts it to a +5 volt pulse for the clock enable. Clock enable flip-flop U11A is set by the leading edge of the data demand and is reset when clock pulse 577 from the clock generator is decoded.

b. ***Clock Generator.*** The clock generator consists of a **2.048** MHz crystal controlled oscillator (U2A). The output of this oscillator is input to a ripple counter (U3) which divides the frequency by 64 for an output of 32 KHz. The clock enable signal allows the clock to run only during the time for one ADAS data block.

c. ***Reset Circuit.*** The reset circuit consists of monostable multivibrator U12A and flip-flop U11B. The flip-flop is used as an inverter to drive the input to the monostable multivibrator. The Q output of the monostable multivibrator is used to reset the word counter. The Q output it used to inhibit the first clock input to the bit enable circuitry.

d. Three Decade ***Counter and Decode.*** The three decade counter, U6, U7, and U8, divides the 32 KHz clock to provide the bit count for the bit counter. The decoder is divided into two sections. The first section, U9A, U9B, U4A, and U5C, decodes the 193rd and 336th counts for the bit inhibit for the BDC data block. The second section, U9C, provides the 577th count to reset the clock enable circuit and to load the count of zero into the bit counter.

e. Bit Counter. The bit counter consists of monostable multivibrator U1A, four bit binary counter U10, and decoders U4B, U4C, and U4D. Monostable multivibrator U1A provides a 300-nanosecond delay of the bit clock for the counter. The binary counter provides the count for the output data selection, the word clock, and bit counter reset. Bits 3 and 5 are decoded by U4B, U4C, and U4D and used to provide the clock for the word counter. Bit 5 is also used to clear the bit counter which counts from 0 through 5.

f. Word Counter. The word counter U13 is a 12-bit binary counter. The clock for the word counter is the decoded third and fifth counts of the bit counter. Consequently, the word counter advances twice for each word at the fourth and sixth bit of the word. The counter is reset at the time of data demand. The seventh bit is one of the inputs to the ramp generator (para 2-93e above).

g. Programable Read Only Memory (PROM) and Data Selection. PROM U14 is a 256-word by 4-bit **PROM** that is programed with the information for a fixed BCD block of data. Each line of data in the data block consists of six bits, of which the first four bits are an even numbered work, i.e., 0,2,4, of the PROM. The remaining two bits are the successive odd word of the PROM i.e., 0, 1, and 2,3. The data selector U15 is a one-of-eight data selector, of which the first six inputs are used. Selection of the six inputs is made by the three control inputs which are driven by the bit counter. The output of the data selector is a single line. The effect is that the word is converted from a parallel six bit word to a serial word. Since the total time for a data bit is approximately 31.25 microseconds, the bit enable circuit controls the inhibit input of the data selector to provide an output pulse of 21 microseconds.

h. Bit Enable *Circuit.* The bit enable circuitry consists of monostable multivibrator U12B, flip-flop Ul7B, and gates Ul6 and U18D. Monostable multivibrator U12B is set for 11 microseconds and is NORed with reset flip-flop U17B. The flip-flop is set by reset monostable multivibrator U12A and is reset by the first bit enable pulse. This is to keep the inhibit on the data selector at the beginning of an ADAS cycle. The output of the gate Ul6C is ANDed with the decoded bits 193 and 386 bit to inhibit the 193rd and 386th output bits of data selector U15.

i. Unblank Level Shifter. Unblank level shifter Q7 and Q8 receive the output of the data selector U15 and convert it from the 5v CMOS level to the 80v pulse required as the unblanking output.

j. BDC/ALT/NUM Selection. The BCD/ALT/NUM selection circuit consists of flip-flop U17A, NOR gates U16B and U16D, and NAND gate U18A. When the ADAS MODE switch is in the BCD mode, the D input of flip-flop U17A is pulled to +5v. The clock to the flip-flop is the data demand. The flip-flop toggles high and enables the ramp generator for every data demand. When the switch is in the ALT mode, the Q output of the flip-flop is connected to the D input and the flip-flop changes state with every data demand. This enables the ramp generator every other data demand. During the data demand that the ramp generator is not enabled, the input to the deflection clock is held low and when the ramp generator is enabled the input to the deflection generator is held high. When the switch is in the NUM mode, the D input of the flip-flop is held at ground. The data demand toggles the flip-flop low. This disables the ramp generator and enables the input to the deflection clock for all data demands.

k. Deflection Clock. The deflection clock consists of monostable multivibrator UlB and level shifting circuitry Q9, Q10, and Q11, which converts the +5 volt CMOS levels to -26 volt to +20 volt levels. The multivibrator is controlled by the reset input. When the reset is held high, the multivibrator is allowed to run. When the reset is held low, the multivibrator is turned *off.*

l. Ramp Generator. Ramp generator consists of U18B, Q2, Q3, Q4, Q5, and Q6. The enable from the BCD/ALT/NUM selection circuit and the 7th bit of the word counter are the inputs to the ramp generator. When both inputs of the gate U18B go high, the output goes low. This turns off Q2, Q3, and Q4 and allows the constant current source Q5 to charge ramp capacitor C12. Output transistor Q6 follows the charge of the capacitor and provides the ramp. The output of the ramp generator and the deflection clock are ORed together to provide the vertical deflection signals.

Section IX. MONITOR ADAPTER INPUT SIMULATOR CIRCUITS, CIRCUIT ANALYSIS

2-94. General

(fig. FO-13)

The monitor adapter input simulator provides ECCM video and ECCM deflection signals which are used to test the monitor display adapter circuits in Recorder-Processor-Viewer, Radar Mapping RO-495/U. The ECCM deflection signal is used for horizontal deflection and is synchronized with the ECCM video signal by a binary counter. The following paragraphs describe the circuits of the monitor adapter input simulator.

2-5. Clock Generator

The clock generator consists of a free-running oscillator (U1). The frequency and duty cycle of the oscillator are controlled by resistors R2 and R3, and capacitor C1. A square wave is produced by selecting a specific ratio of resistors R2 and R3. A 13-kHz square wave clock signal is generated and applied to the binary counter (U2).

2-96. Binary Counter

Counter (U2) is a 4-bit binary synchronous counter which counts from zero through 15 and then recycles. A buffered clock input triggers the 4 internal flip-flops on the positive-going edge of the 13-kHz clock generator signal when enabled by internal gating. Binary counter outputs are routed to the video decoder, deflection decoder, and the ramp generator.

2-97. Ramp Generator

The ramp generator consists of a level changer (Q5, Q4), switch circuit (Q3), and operational amplifier (U6). The "D" output of the binary counter is applied to the emitter of transistor Q5. A logic high occurs at the "D" output during the binary counts of 8 through 15. This voltage corresponds to a negative level voltage at the collector of transistor Q4, and is applied to the gate (G) of JEET (Q3). Q3 is cut off and effectively opens the dc feedback path between the output of U6 and the input of U6 (inverting). Capacitor C3 then begins to charge through R17 and causes in increasing negative voltage on the output of U6. During counts of zero through 7, a positive voltage is applied to the gate of JFET Q3. Q3 conducts and capacitor C3 discharges through Q3 at a fast rate causing the negative voltage at the U6 output to increase to its starting voltage level.

2-98. Video Decoder

The video decoder consists of a gate (U3A), inverter (U4F), and level changer (Q1, Q2). The "A" and "D" outputs of the binary counter are applied to the input of U3A. During binary counts 9, 11, 13, and 15, a logic high occurs at the "A" and "D" outputs, producing a logic low at the gate output (U3A). Binary counts other than 9, 11, 13, and 15 produce a logic high at U3A output. The output of U3A is applied to the input of inverter (U4F). The function of the level changer (Q1, Q2) is to change the positive voltage to a negative voltage level. The level changer (Q2) is routed to connector J10 as the ECCM video signal.

2-99. Deflection Decoder (fig. 2-20)

The deflection decoder consists *of 5* inverters (U4A through U4E) and 3 gates (U3B, U3C, and U3D). The following timing diagram shows the binary counter output logic applied as input to the decoder and the decoder output which is applied to the summer circuit.

2-100. Summer

The summer consists of an operational amplifier (U7) and current buffer (U8). Operational amplifier (U7) provides for a composite waveform of the output of the ramp generator and the deflection decoder. The

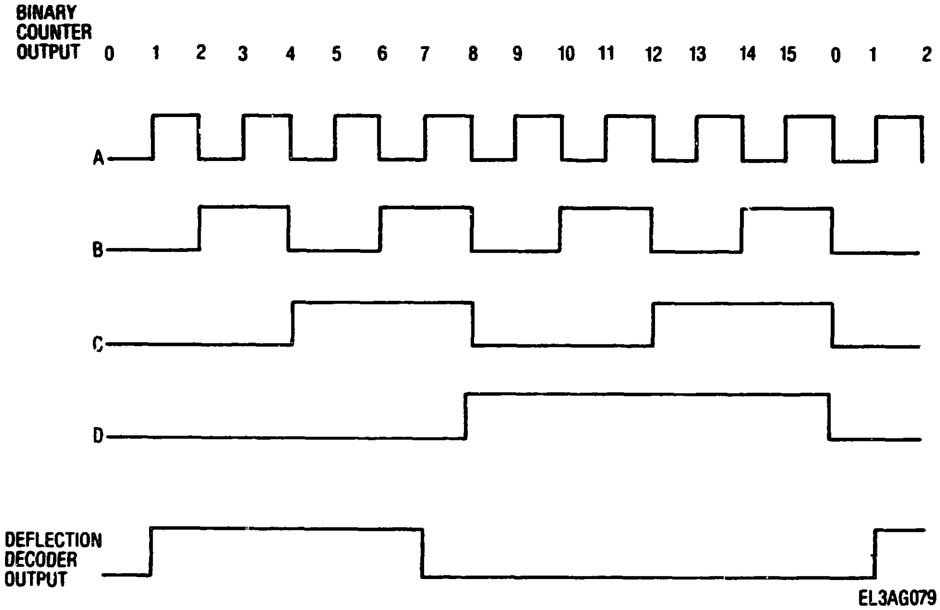


Figure 2-20. Deflection coder, timing diagram.

ramp generator signal is applied to the inverting input of U7. The deflection decoder waveform is applied to the inverting input of U7. The deflection decoder waveform is applied to the non-inverting input of U7. The summed composite signal output of U7 consists of a positive-going ramp voltage (binary counter counts 8 through 15), followed by a low level voltage (binary counter count zero). This is followed by a positive-going pulse (binary counter counts 1 through 6), followed by a low level voltage (binary counter count 7). The U7 output waveform is applied to the input buffer U8. U8 is used as a current source for external load requirements. The U8 output is routed to connector J11 as the ECCM deflection signal.

CHAPTER 3

DIRECT SUPPORT MAINTENANCE INSTRUCTIONS

Section I. INTRODUCTION

3-1. Scope of Direct Support Maintenance

This chapter contains the following direct support maintenance functions for the test set group; bench testing, troubleshooting, removal and replacement procedures, repair procedures, cleaning, painting, calibration, physical tests and inspection, and electrical testing. The direct support maintenance procedures supplement the maintenance procedures contained in TM 11-6625-1833-12.

3-2. Organization of Direct Support Maintenance

The maintenance duties assigned to direct support maintenance personnel are listed in a through j below together with references to the paragraphs covering the specific maintenance function.

a. Connector continuity checks (pars 3-11 through 3-14).

b. Bench tests (para 3-16 through 3-33).

c. Troubleshooting (para 3-16 through 3-33).

d. Removal and replacement procedures (para *3-36)*.

e. Cable repair (para 3-37).

f. Cleaning (para 3-38).

g. Painting (para 3-39).

h. Calibration (para 3-40 through 3-43).

i. Physical tests and inspection (para 3-45 **through** *3-48)*.

j. Electrical tests (para 3-49).

3-3. Tools and Test Equipment Required for Direct Support Maintenance

The tools and test equipment required to perform direct support maintenance on the test set group are listed in table 3-l below.

Table 3-1 . Tools and Test Equipment

Test Equipment	Technical Manual	Common Name
Multimeter AN/USM-223	TM 11-6625-366-15	Multimeter
Oscilloscope AN/USM-281C	TM 11-6625-2658-14	Oscilloscope
Transformer, Variable Power, General Radio Type M-2G3		Variable transformer
Voltmeter, Digital AN/GSM-64B	TM 11-6625-444-14-1	Digital voltmeter
Generator, Signal SG-1105/G		Pulse generator
Tool Kit, Electronic Equipment TK-105/G	SC-5180-91-CL-R07	Toolkit
Termination, 100-ohm HP10100B		100-ohm termination

Section II. TROUBLESHOOTING

WARNING

In normal operation, testing, and troubleshooting of the test set group, voltages up to +640 volts at power levels sufficient to cause DEATH on contact may be present. It is imperative that all warning notices in each particular procedure be observed and instructions complied with step by step.

3-4. General

a. Troubleshooting at direct support maintenance level includes all the techniques outlined for organizational maintenance and any special or additional techniques required to isolate a malfunction to a defective part. The direct support maintenance procedures are not complete in themselves but supplement the procedures outlined in TM 11-6625-1833-12.

b. When trouble in the equipment occurs, certain observations, tests, and measurements can be made that will aid maintenance personnel in localizing the malfunction to a particular part. The test procedures in this section are used to verify any malfunction or trouble symptom reported by lower category of maintenance. Additional troubleshooting techniques are described in detail in paragraphs 3-6 through 3-10.

3-5. Organization of Troubleshooting Procedures

a. Troubleshooting the equipment consists of performing a bench test on the equipment to determine any malfunction within the equipment. The bench tests in this section are arranged in a systematic manner and should be followed sequentially as applicable. If, however, maintenance personnel desire to perform any test within this section, it is necessary to perform the preliminary procedures first.

b. Each bench test in this section is keyed to an associated troubleshooting table. In addition, each trouble symptom listed in the troubleshooting table is also keyed to a particular step in the associated bench test. This technique is used with all the troubleshooting procedures in this section to localize a fault to a defective component, subassembly, or module. After localization of a defective component, subassembly, or module, it is replaced and the defective part is forwarded to a higher category of maintenance.

c. The schematic and wiring diagrams contained in this technical manual should be used by maintenance personnel as aid when troubleshooting the equipment. The wire lists in section V provide point-to-point (from and to) data of each wire within the test set group. This listing is presented in alpha-numeric sequence format including a designated identifying wire number.

d. Continuity checks for each front panel connector is provided in paragraphs 3-11 through 3-14. Checking continuity of test set group cables is given in paragraph 3-37.

3-6. Troubleshooting with BITE

The test set group contains built-in test equipment (BITE) to alert the equipment operator when a malfunction occurs and to provide maintenance personnel with a means for determining the major circuit group in which a malfunction has occurred. The BITE circuit is enabled when the BITE switch is in the ON position. A failure indication detected by BITE circuitry causes the FAILURE indicator lamp on panel 1A2 to light. Paragraph 3-7 lists the circuits whose failure will light the FAILURE indicator lamp.

3-7. FAILURE Light Indications

The FAILURE indicator lamp will light if an overvoltage or undervoltage condition exists in a horizontal sweep, vertical sweep, sweep video, or unblank circuit. When this indicator lamp is lit, refer to the troubleshooting procedure for the following circuits:

a. Horizontal sweep troubleshooting, (para 3-25).
b. Vertical sweep troubleshooting, (para 3-24).
c. Video compression troubleshooting, (para 3-28).
d. Unblank circuit troubleshooting, (para 3-26).

3-8. SWEEP FAULT Light Indications

This lamp will flash when a fault exists in video amplifier lA2A6, sweep generator 2A4, or horizontal amplifier 2A2. Refer to paragraphs 3-24,3-25, and 3-28 for troubleshooting these circuits.

3-9. INDICATOR FAULT Light Indications

This lamp will flash when a fault exists in the indicator fault line.

3-10. SERVO FAULT light Indications

a. This lamp will flash when a fault exists in one or more of the following circuits:

(1) Servoamplifier 2A5.

(2) Servo loop circuits (synchros, drive gears, reduction gears, etc.).

b. For localizing the fault to a specific circuit or component, refer to paragraph 3-19 or 3-20.

3-11. Connector Continuity Test

a. General. The following tests are to be performed on all multipin electrical connectors of the test set group. Most panel mounted multipin connectors have an array of numbered test points located adjacent to the connector. There is one test point in an array for each associated connector pin. The test points associated with rectangular shaped multipin connectors are numbered to correspond to the number of the connector pin to which they are connected. The test points associated with the round shaped multipin connectors are also numbered but the test point numbers in the array do not correspond to the connector pin designations in their associated connectors since the connector pins are lettered. A cross-reference between test point numbering and connector pin lettering is provided in table 3-2.

NOTE

Some connectors do not contain all 41 pins listed in table 3-2.

b. Test Equipment Required. The only test equipment required for the connector continuity test is Multimeter AN/USM-223.

c. Test Connections and Conditions.

(1) The continuity tests are performed with the test set group disconnected from all other equipment.

(2) Perform the continuity tests (para 3-12 through 3-14). Connect the multimeter as directed in the test procedures. Refer to the wire list in paragraphs 3-51, 3-52, 3-53 if abnormal measurement indications are encountered.

Table 3-2. Test Point-Connector Pin Cross-Reference

Test Point No.	Connector Pin Letter	Test Point No.	Connector Pin Letter	Test Point No.	Connector Pin Letter
1	A	15	R	29	f
2	B	16	S	30	g
3	C	17	T	31	h
4	D	18	U	32	i
5	E	19	V	33	j
6	F	20	W	34	k
7	G	21	X	35	m
8	H	22	Y	36	n
9	J	23	Z	37	p
10	K	24	a	38	q
11	L	25	b	39	r
12	M	26	c	40	s
13	N	27	d	41	t
14	P	28	e		

3-12. Indicator Simulator (Unit 1A1) Connector Continuity Procedure

a. LOW VOLTAGE POWER SUPPLY Connector Jl. Refer to table 3-2 and measure the resistance between the test points and associated pins of connector Jl with the multimeter. All resistance measurements should be less than 0.5 ohm, except those made at test points *4*, 5, 7, 9, 16, 17, and 19 through 26. Measurements made at these test points should indicate infinite resistance.

b. HIGH VOLTAGE REGULATOR Connector J2. Refer to table 3-2 and measure the resistance between the test points and associated pins of connector J2 with the multimeter. All resistance measurements should be less than *0.5* ohm, except those made at test points 4, 5, 7, 8, 9, 10, 25, and 27 through 41. Measurements made at these test points should indicate infinite resistance.

c. METERING ROLLER DRIVE Connector J3. Refer to table 3-2 and measure the resistance between the test points and associated pins of J3 with the multimeter. All resistance measurements should be less than 0.5 ohm except those made at test points 16, 17, 18, and 19. Measurements made at these test points should indicate infinite resistance.

d. RACK/RO-495/U Connector J4. Refer to table 3-2 and measure the resistance between the test points and associated pins of J4 with the multimeter. All resistance measurements should be less than 0.5 ohm except those made at test points 5, 8, 21, 22, 23, 26, 27, 32 through 38, and 40. Measurements made at these test points should indicate infinite resistance.

e. HIGH VOLTAGE SUPPLY Connector J5. Refer to table 3-2 and measure the resistance between the test points and associated pins of connector J5 with the multimeter. All resistance measurements should be less than 0.5 ohm except those made at test points 4, 5, 6, 7, 15, 16, 17, 20, 21, and 26. Measurements made at these test points should indicate infinite resistance.

f. ADAS SIMULATOR Connector J7. Refer to table 3-2 and measure the resistance between the test points and associated pins of J7 with the multimeter. All resistance measurements should be less than 0.5 ohm except those made at test points 2, 4 through 11, 13, 14, and 16. Measurements made at these test points should indicate infinite resistance.

g. ADAS DEMAND Connector J9. Refer to table 3-2 and measure the resistance between the test points and associated pins *of* connector J9 with the multimeter. All resistance measurements should be less than 0.5 ohm except those made at test points 3, 5, and 7 through 10. Measurements made at these test points should indicate infinite resistance.

3-13. Indicator Simulator (Unit 1A2) Connector Continuity Procedure

a. YOKE *DRIVE Connector* Jl. Refer to table 3-2 and measure the resistance between the test points and associated pins of connector Jl with the multimeter. All resistance measurements should be less than 0.5 ohm.

b. RACK/SWEEP Connector J10. Measure the resistance between the test points and associated pins of connector J10 with the multimeter. All resistance measurements should be less than 0.5 ohm, except those made at test points 52,68,89 through 92,94,95, and 100. Measurements made at these test points should indicate infinite resistance.

c. INDICATOR/SWEEP Connector- *J11.* Measure the resistance between the test points and associated pins of connector J11 with the multimeter. All resistance measurements should be less than 0.5 ohm, except those made at test points, 6,12,19,20,25,26, 31,34,48,53,56,60,62, and 63. Measurements made at these test points should indicate infinite resistance.

d. YOKE LOAD Connector *J14.* Refer to table 3-2 and measure the resistance between the test points and associated pins of connector J14 with the multimeter. All resistance measurements should be less than 0.5 ohm.

e. HIGH VOLTAGE REGULATOR Connector J15. Refer to table 3-2 and measure the resistance between the test points and associated pins of connector J15 with the multimeter. All resistance measurements should be less than 0.5 ohm, except those made at test points 4, 5, 7 through 10, 25, and 27 through 41. Measurements made at these test points should indicate infinite resistance.

f. Connector J16. This connector is not used.

g. NAV SIM/RACK Connector J18. Refer to table 3-2 and measure the resistance between the test points and associated pins of connector J18 with the multimeter. All resistance measurements should be less than 0.5 ohm, except those made at test points 11 and 12. Measurements made at these test points should indicate infinite resistance.

h. ADAS/RACK Connector J20. J20. Refer to table 3-2 and measure the resistance between the test points and associated pins of connector J20 with the multimeter. All resistance measurements should be less than 0.5 ohm, except those made at test points 7 through 10. Measurements made at these test points should indicate infinite resistance.

i. I BOX/RACK Connector *J22.* Refer to table 3-2 and measure the resistance between the test points and associated pins of connector J22 with the multimeter. All resistance measurements should be less than 0.5 ohm, except those made at test points 1, 10, and 11. Measurements made at these test points should indicate infinite resistance.

j. RCDR/RACK Connector J24. Refer to table 3-2 and measure the resistance between the test points and associated pins of connector J24 with the multimeter. All resistance measurements should be less than 0.5 ohm, except those made at test points 21,22, 23,27,34, and 40. Measurements made at these test points should indicate infinite resistance.

k. RGP/RACK **Connector** *J26.* Refer to table 3-2 and measure the resistance between the test points and associated pins of connector J26 with the multimeter. All resistance measurements should be less than 0.5 ohm, except those made at test points 8,17, 18, and 20. Measurements made at these test points should indicate infinite resistance.

3-14. Generator Simulator (Unit 2) Connector Continuity Procedure

a. SWEEP/INDICATOR Connector Jl. Measure the resistance between the test points and associated pins of connector Jl with the multimeter. All resistance measurements should be less than 0.5 ohm, except those made at test points 19,20,25,26,31,34, 48,53,56,60,62, and 63. Measurements made at these test points should indicate infinite resistance.

b. SWEEP/RACK Connector J2. Measure the resistance between the test points and associated pins of connector J2 with the multimeter. All resistance measurements should be less than 0.5 ohm, except those made at test points 52,68,84,89,90,91,92,95, and 100. Measurements made at these test points should indicate infinite resistance.

c. SWEEP CONTROL Connector J3. Measure the resistance between the test points and associated pins of connector J3 with the multimeter. All resistance measurements should be less than 0.5 ohm, except those made at test points 89, 90, 91, 92, 98, 99, and 100. Measurements made at these test points should indicate infinite resistance.

d. CONTROL/SWEEP Connector J4. Measure the resistance between the test points and associated pins of connector J4 with the multimeter. All resistance measurements should be less than 0.5 ohm, except those made at test points 89 through 92, 94, and 98 through 100. Measurements made at these test points should indicate infinite resistance.

e. LOW VOLTAGE POWER SUPPLY Connector J5. Refer to table 3-2 and measure the resistance between the test points and associated pins of connector J5 with the multimeter. All resistance measurements should be less than 0.5 ohm, except those made at test points 4, 5, 7, 9, 17, and 19 through 26. Measurements made at these test points should indicate infinite resistance.

3-15. Test Set Group Functional Tests (fig. FO-4)

a. General. The following tests are required to electrically test the test set group. A basic test setup is used for all testing. Modifications to this test setup are described in individual test procedures. Each test is associated with a troubleshooting table which immediately follows the test. Primary power required for test set group operation is 115 vac, 400 Hz and +28 vdc.

b. Tools and Test Equipment Required. The tools and test equipment listed in table 3-l are required for the test set group functional tests.

c. *Basic Test Setup.* Remove all cables stored in the upper cover of the generator simulator. Prepare the test set group for the functional tests as follows:

(1) Arrange the equipment on a suitable workbench in the following left-to-right order: indicator simulator (unit lA2), generator simulator (unit 2), and indicator simulator (unit 1Al).

(2) Open (pull out) AC, DC, LOW VOLTAGE circuit breakers on unit lA2.

(3) Connect interconnecting cables to the test set group as illustrated in figure FO-4. Additions and/or modifications are given in individual test procedures.

(4) Set all switches and controls to the off, down, or fully counterclockwise position.

d. Initial Test Equipment Calibration

(1) Apply power to the oscilloscope,, digital voltmeter, variable transformer, and pulse generator and allow a 15 minute warmup period prior to performing tests

(2) After the test equipment has warmed up, adjust the variable transformer for 115-volt ac output (line to neutral) using the digital voltmeter.

e. Initial Waveform Instructions.

(1) For all waveform displays, connect the A input of the oscilloscope as directed by the test procedure and the low or ground terminal of the oscilloscope to chassis ground.

(2) The oscilloscope may be triggered internally or the SWEEP GATE output jack 1A2J8 may be connected externally to trigger the oscilloscope to obtain a readable display during testing.

(3) Waveforms are presented for the conditions specified in the test procedures and waveform illustrations.

WARNING

When power is applied to the test set group, potentials in excess of +640 vdc, +100 vdc, and 115 vac exist in Test Set Subassembly MX-8638A/APS-94D and potentials of +640 and -531 vdc exist throughout the test set group. Exercise extreme caution when power is applied to avoid contact with any exposed connector terminals. Contact with these voltages may result in injury or DEATH.

NOTE

Each test in this section is organized in a systematic manner to assure that a complete test is performed. Connect the test equipment as directed in the test procedure. The tests are arranged to be performed in the sequence given. Should a random test be performed, make sure that all the preliminary steps given in paragraph 3-15 above have been accomplished.

3-16. Primary Power Distribution Trouble-Shooting

a *Bench* Test. Perform the primary power distribution bench test as described in table 3-3 below.

Table 3-3 Primary Power Distribution Test

Step No.	Control Settings: Test Equipment	Control Settings: Equipment Under Test	Test Procedure	Performance Standard
1	None	Unit 1A2; DC RESET: Press Down; AC RESET· Press Down; Unit 2· POWER: ON	Verify that the blower motor in unit 1A1 ·s not run.	Blower motor does not run in unit 1A1.
2	Digital voltmeter Power: ON RANGE. AUTO FUNCTION: VAC		After a 2 minute warmup, measure the voltage level between the following test points	
			a 1A2J11-57 and 2J2-56	*a* 115 ± 10 vac
			b 1A2J11-58 and 2J2-56	*b* 115 ± 10 vac
			c 1A2J11-59 and 2J2-56 .	*c* 115 ± 10 vac
		Unit 1A2 LOW VOLTAGE RESET Press down	*d* 1A1J1-1 and 2J2-56	*d* 115 ± 10 vac
			e 1A1J1-2 and 2J2-56 .	*e* 115 ± 10 vac
			f 1A1J1-3 and 2J2-56	*f* 115 ± 10 vac
			g Verify that the blower motor in unit 1A1 is operating.	*g* Blower motor operating
			h 2J4-1 and 2J4-2 . .	*h* 26 ± 2 vac
3	Digital voltmeter RANGE AUTO FUNCTION: VDC		Measure the voltage level between the following test points	
			a 1A1J2-18 (+) and 1A1J2-19 (-)	*a* +28 ± 2 vdc
			b 2J4-22 (+) and 2J4-23 (-)	*b* +28 ± 2 vdc
			c 2J4-22 (+) and 1A2J20-12 (-)	*c* +28 ± 2 vdc
			d 2J4-12 (+) and 1A2J20-12 (-)	*d* +28 ± 2 vdc
			e 1A2J22-19 (+) and 1A2J15-19 (-)	*e* +28 ± 2 vdc
			f 1A2J10-υ9 (+) and 1A2J11-27 (-)	*f* +28 ± 2 vdc
4	Digital voltmeter RANGE: AUTO FUNCTION: VAC	Unit 1A2 ILLUM ON	Measure voltage level between the following test points 2J4-3 and 2J4-101	4 8 ± 0 4 vac

b. Troubleshooting Procedure. The following procedure is used when a fault is suspected in the primary power distribution circuits of the test set group. Primary power is defined as the distribution of the 115 *vac,* 400 Hz, 3-phase and 28 vdc bench power in the test set group. Figure FO-5 shows the primary power distribution and control system of the test set group and will be an aid to the technician when troubleshooting.

Table 3-4. Primary Power Distribution Troubleshooting

Item No.	Trouble Symptom	Probable Trouble	Checks and Corrective Actions
1	115 vac not present at test points 1A1J1-1, -2, and -3 (all measurements referenced to neutral line test point 2J2-56).	*a.* AC RESET circuit breaker on panel 1A2 is open *b* LOW VOLTAGE RESET circuit breaker on panel 1A2 is open *c.* Defective wiring or connectors *d.* 1A2K1 inoperative *e* Defective overvoltage protector module 1A2A5.	*a.* Reset circuit breaker. *b* Reset circuit breaker. *c* Measure for 115 vac at test points 1A2J22-3, -4, and -5 referenced to test point 1A2J22-6 If present, defective wiring is indicated Check wiring Refer to wiring lists (section V) If voltage is not present, measure for presence at bench input to the test set group. *d* Check for presence of 28 vdc at test point 1A2J22-19 (referenced to ground at 2J3-23) If present, chassis 1A2 must be removed and relay 1A2K1 checked, remove and replace if defective (fig. 3-8) NOTE: Relay 1A2K1 is operative if the POWER ON light on panel 1A2 is illuminated or the blower motor of panel 1A1 is operating *e* Replace overvoltage protector module 1A2A5 (fig 3-7)
2	Blower motor inoperative.	*a.* AC RESET circuit breaker on panel 1A2 is open *b* LOW VOLTAGE RESET circuit breaker on panel 1A2 is open. *c* Defective wiring or connectors *d.* Defective blower motor	*a.* Reset circuit breaker *b* Reset circuit breaker *c* Same as item 1*c* above *d* Replace blower motor
3	With the POWER switch of unit 2 in the ON position, +28 ±2 vdc is not present at any of the following test points. *Test Point* ... *Reference* 1A1J2-18 ...... 1A1J2-19 2J4-22 .... 2J4-23 2J4-22 .... 1A2J20-12 2J4-12 .... 1A2J20-12 1A2J22-19 .... 1A2J15-19	*a.* Open DC RESET circuit breaker on 1A2 panel. *b* Defective wiring W10 or connector 1A2J12	*a.* Reset the circuit breaker *b* Check wiring Refer to wiring lists paras 3-51, 3-52, and 3-53
4	+28 vdc not present at test point 1A2J10-59 (referenced to 28 vdc return at test point 1A2J11-27) or not within ±0.05 vdc tolerance, test points of 3 above are normal	*a* Defective low voltage power supply and regulator 1A2A3 *b* Defective wiring or connector	*a* Replace 1A2A3 (fig 3-7) If still abnormal, proceed to *b* below *b* Check wiring Refer to wiring lists paras 3-51, 3-52, and 3-53.
5	28 vdc not present at one or more of the test points given in 3 above At least one test point indicates normal voltage	Defective wiring or connector	Check wiring Refer to wiring lists (paras 3-51, 3-52, and 3-53)
6	4.8 vac not present between test points 2J4-3 and 2J4-101.	*a* AC RESET circuit breaker on panel 1A2 is open. *b* LOW VOLTAGE RESET circuit breaker on panel 1A2 is open	*a* Reset circuit breaker *b* Reset circuit breaker

Table 3-4. Primary Power Distribution Troubleshooting - Continued

Item No.	Trouble Symptom	Probable Trouble	Checks and Corrective Actions
		c. Defective wiring or connector	*c.* Check wiring. Refer to wiring lists (paras 3-51, 3-52, and 3-53).
		d. 1A2K1 relay inoperative.	*d.* Replace 1A2K1 relay (fig. 3-8).
		e. Defective transformer 1A1T2.	*e.* Replace transformer 1A1T2.
		f. Defective switch 1A2S1.	*f.* Replace switch 1A2S1.
7	26 vac not present between test points 2J4-1 and 2J4-2.	*a.* AC RESET circuit breaker on panel 1A2 is open.	*a.* Reset circuit breaker.
		b. Defective transformer 1A1T2.	*b.* Replace transformer 1A1T2.

3-17. Low Voltage Power Supplies Troubleshooting

a. Bench Test. Perform the low voltage power supplies test as described in table 3-5 below. Refer to figure FO-6 for location of test points in units 1A1 and 1A2.

WARNING

Dangerous voltages exist in these circuits. Use extreme care when making voltage measurements.

Table 3-5. Low Voltage Power Supplies Test

Step No.	Control Settings		Test Procedure	Performance Standard
	Test Equipment	Equipment Under Test		
1	Digital voltmeter: RANGE: AUTO FUNCTION: VDC	None	Measure voltage level between the following test points: *a.* 1A1J1-8 (+) and 1A1J1-14 (-) *b* 1A1J1-6 (-) and 1A1J1-14 (+) *c.* 1A1J1-10 (-) and 1A1J1-14 (-) *d.* 1A1J1-11 (+) and 1A1J1-14 (-) *e.* 1A1J1-12 (+) and 1A1J1-14 (-) *f* 1A1J1-13 (+) and 1A1J1-14 (-) *g* 1A1J1-18 (+) and 1A1J1-14 (-)	 *a.* +20 0 ±0.2 vdc. *b.* -20.0 ±0.2 vdc. *c.* -28.0 ±1.0 vdc. *d* +6 3 ±0.2 vdc. *e* +101 ±3.0 vdc. *f* +640 ±40.0 vdc. *g* +531 ±12.5 vdc.
2	Digital voltmeter: RANGE. AUTO FUNCTION: VDC	None	*a.* Remove 18 screws from the front panel of Unit 1A1. *b* Remove panel 1A1 from the cabinet *c* Place the +28 volt regulated power supply and high voltage loads card (1A1A2) on extender. *d.* Measure voltage level between the following test points: (1) 1A1J3-1 (+) and 1A1J3-2 (-) (2) 1A1J4-6 (+) and 1A1J4-7 (-) (3) 1A1A2-T (+) and 1A1A2-1 (-) *e* Remove card 1A1A2 from the extender and replace back in panel 1A1	*a* None. *b* None. *c* None. *d* Voltages should be as follows: (1) +28.0 ±2.0 vdc. (2) +28.0 ±2.0 vdc. (3) + 5.0 ±0.2 vdc. *e* None
3	Digital voltmeter: RANGE: AUTO FUNCTION: VDC	Unit 1A1: HIGH VOLTAGE ON	Measure voltage level between the following test points. 1A1J5-1 (+) and 1A1J5-2 (-).	26.00 ±0.030 vdc
4	Digital voltmeter. RANGE: AUTO FUNCTION: VDC	Unit 1A2: VERTICAL OFFSET OVERRIDE. ON	*a* Place the low voltage power supply regulator card (1A2A3) on extender *b* Measure voltage level between the following test points: (1) 1A2J24-39 (+) and 1A2J11-27 (-)	*a.* None *b* Voltages should be as follows: (1) +20 ±0.5 vdc

Table 3-5. Low Voltage Power Supplies Test - **Continued**

Step No.	Control Settings: Test Equipment	Control Settings: Equipment Under Test	Test Procedure	Performance Standard
			(2) 1A2A3-J (+) and 1A2A3-1 (-) (3) 1A2A3-V (+) and 1A2A3-1 (-) (4) 1A2A3-4 (-) and 1A2A3-1 (+) *c*. Remove card 1A2A3 from the extender and replace back in panel 1A1. *d* Replace panel 1A2 back in cabinet. *e* Replace 18 screws on the front panel of 1A1	(2) +28 ±2 0 vdc (3) + 5 ±0.2 vdc (4) - 5 ±0 2 vdc *c* None *d* None *e* None
5	Digital voltmeter: RANGE: AUTO FUNCTION: VDC	None	Measure voltage level between the following test points *a*. 1A1J2-16 (+) and 1A1J2-11(-) *b* 1A1J2-17 (-) and 1A1J2-11 (+)	 *a* +15 ±0 2 vdc *b* -15 ±0 2 vdc

b. Troubleshooting Procedure. The following procedure is used in troubleshooting the low voltage system of the test set. Secondary power distribution and control circuits are shown in figure FO-6 and will be an aid to the rapairman when troubleshooting.

WARNING

Dangerous voltages exist in the low voltage power supply circuits. Use extreme care when troubleshooting these circuits.

Table 3-6. Low Voltage Power Supply Troubleshooting

Item No	Trouble Symptom	Probable Trouble	Checks and Corrective Actions
1	Abnormal or no voltage measured at one or more of the following test points (referenced to signal ground at test point 1A1J1-14): 1A1J1-8 (+20 vdc) 1A1J1-6 (-20 vdc) 1A1J1-10 (-28 vdc) 1A1J1-11 (+6.3 vdc) 1A1J1-12 (+100 vdc) 1A1J1-13 (+640 vdc) 1A1J1-18 (+531 vdc)	*a*. AC RESET or LOW VOLTAGE RESET circuit breaker on unit 1A2 open. *b* Defective low voltage power supply 1A1A3 *c* Defective low voltage regulator 1A1A4	*a* Reset circuit breaker and retest for corrective voltages *b* Check for presence of 115 vac at test points 1A1J1-1, -2, and -3 referenced to neutral at test point 2J2-56 If present, replace low voltage power supply 1A1A3 (fig 3-4) If not present, refer to the primary power distribution troubleshooting procedures (para 3-16) *c* Replace low voltage regulator 1A1A4 (fig 3-3)
2	Abnormal or no voltage measured at one or more of the following test points (referenced to ground at test point 1A2J22-23) 1A2J24-15 (+20 vdc) 1A2J16-10 (+28 vdc) 1A2J24-39 (+20 vdc)	*a*. AC RESET circuit breaker on unit 1A2 open *b* Relay 1A2K1 defective or inoperative *c* Defective low voltage power supply and regulator 1A2A3	*a* Reset circuit breaker *b* Check for presence of +28 vdc at test point 1A2J22-19 (referenced to ground at test point 2J3-23) If present, chassis 1A2 must be removed and 1A2K1 checked, remove and replace if defective (fig 3-8) **NOTE:** Relay 1A2K1 is operative if the POWER ON light on panel 1A2 is illuminated or the blower motor of panel 1A1 is operating *c* Replace the low voltage power supply and regulator 1A2A3 (fig 3-7)
3	Abnormal or no +28 vdc regulated voltage at the test point 1A1J4-6 (referenced to ground)	AC RESET or LOW VOLTAGE RESET circuit breaker on unit 1A2 open	Reset circuit breaker

Table 3-6. Low Voltage Power Supplies Troubleshooting - Continued

Item No.	Trouble Symptom	Probable Trouble	Checks and Corrective Actions
4	Abnormal or no voltage measured at one or more of the following connector pins (referenced to signal ground at pin 1 of connector (1A2A3): 1A2A3–E (+20 vdc) 1A2A3–J (+28 vdc) 1A2A3–V (+ 5 vdc) 1A2A3–4 (– 5 vdc)	Defective low voltage power supply and regulator.	*a.* Check for presence of 26 vac between pins 1A2A3–A, 1A2A3–B, and 1A2A3–C. *b.* Check for presence of 7.4 vac between pins 1A2A3–K, 1A2A3–L, and 1A2A3–M. *c* Check for presence of 8.1 vac between pins 1A2A3–20, 1A2A3–21, and 1A2A3–22. *d* If above voltages are present replace the low voltage power supply and regulator (fig 3–4). If not present, refer to the primary power distribution troubleshooting procedures (para 3–16).
5	Abnormal or no voltage measured at one or more of the following connector pins (referenced to signal ground at pin 1 of connector 1A1A2) 1A1A2–Y (+28 vdc) 1A1A2–S (+28 vdc) 1A1A2–20 (+28 vdc) 1A1A2–T (+ 5 vdc)	Defective +28 volt regulated power supply and high voltage loads.	Check for presence of 43 vac between pins 1A1A2–18 and 1A1A2–V. If present, replace the +28 volt regulated power supply and high voltage loads (fig. 3–4) If not present, refer to figure FO–5
6	Abnormal or no voltage measured at one or more of the following test points (referenced to ground at test point 1A1J2–11): *a.* 1A1J2–16 (+15 vdc).	*a* One or more of the following components defective: (1) Offset amplifier (2A6) (2) Regulator transistor 2Q1 (3) Low voltage power supply 1A1A3	*a* Replace one or more of the following components: (1) Offset amplifier 2A6 (fig. 3–12). (2) Regulator transistor 2Q1 (fig. 3–12). (3) Check for presence of 115 vac at test points 1A1J1–1, –2, and –3 referenced to neutral at test point 2J2–56. If present, replace low voltage power supply 1A1A3 (fig 3–4). If not present, refer to primary power distribution troubleshooting procedures (para 3–16).
	b 1A1J2–17 (-15 vdc)	*b.* Same as item 6*a* above	*b* Same as item 6*a* above.
7	26 vdc not present at test points 1A1J5–1 (+) and 1A1J5–2 (-).	*a.* +28 vdc not present at 1A2J2–18. *b* Defective power supply 1A1PS1	*a* Refer to primary power troubleshooting (para 3–16). *b* Replace power supply 1A1PS1 (fig. 3–4).

3-18. Panel Lights Troubleshooting

a. ***Bench*** Test. Perform the panel lights bench test as described in table 3-7 below.

Table 3-7. Panel Lights Test

Step No	Control Settings: Test Equipment	Control Settings: Equipment Under Test	Test Procedure	Performance Standard
1	None	Unit 2 PANEL LIGHTS TEST	Observe all panel lights on this unit	All lights illuminate
2	None	Unit 1A2 PANEL LIGHTS TEST	Observe all panel lights on this unit	All lights illuminate

Table 3-7. Panel Lights Test - Continued

Step No.	Control Settings: Test Equipment	Control Settings: Equipment Under Test	Test Procedure	Performance Standard
3	None	None	Observe POWER on lamps on unit 1A2 and unit 2.	All lights illuminate.
4	None	Unit 1A1: HIGH VOLTAGE power supply: ON	Observe HIGH VOLTAGE panel light on this unit.	Light illuminate
5	None	Unit 1A1: Jumper between test points 1A1J4–6 and 1A1J4–13	Observe MAP ON panel light on this unit.	Light illuminates

b. Troubleshooting Procedure. The following procedure is used in troubleshooting the panel lights on the test set group.

Table 3-8. Panel Lights Troubleshooting

Item No.	Trouble Symptom	Probable Trouble	Checks and Corrective Actions
1	HIGH VOLTAGE ON lamp on panel 1A1 fails to light when HIGH VOLTAGE switch of panel 1A1 is operated to ON position.	Defective HIGH VOLTAGE switch 1A1S2.	Check HIGH VOLTAGE switch (fig 3–3) and replace if necessary.
2	Panel lights fail to light when PANEL LIGHTS switch on panel 1A2 or panel 2 is set to TEST.	*a.* Unit 2. Defective switch S10. *b* Unit 1A2. Defective switch S2.	*a.* Replace switch S10 (fig 3–11) *b.* Replace switch S2 (fig. 3–16)
3	POWER ON lamps on panel 1A2 or 2 fail to light.	Defective relay 1A2K1.	Check for presence of +28 vdc at test points 1A2J22–19 (referenced to ground at 2J3–23). If present, and POWER ON lamp fails to light, chassis 1A2 must be removed and relay 1A2K1 checked (fig 3–8)
4	MAP ON lamp on panel 1A1 fails to light.	Defective lamp.	Replace lamp

3-19. Servo Loop Troubleshooting

a. *Bench* Test. Perform the servo loop bench test as described in table 3-9 below.

Table 3-9. *Servo Loop Test*

Step No.	Control Settings: Test Equipment	Control Settings: Equipment Under Test	Test Procedure	Performance Standard
1	None	Unit 2 NAVIGATION AUTO SERVO LOOP GS GS/DFT DRIVE ON Unit 1A2 NAV SIM. 15R	Observe GS/DFT indicator dial and SERVO FAULT indicator lamp on unit 2	GS/DFT indicator dial nulls and SERVO FAULT indicator lamp is extinguished
2	None	Unit 2. GS/DFT DRIVE OFF UNIT 1A2 NAV SIM· 10R	Same as 1 above	GS/DFT indicator dial does not null and SERVO FAULT indicator lamp flashes

Table 3-9. Servo Loop Test - Continued

Step No.	Control Settings: Test Equipment	Control Settings: Equipment Under Test	Test Procedure	Performance Standard
3	None	Unit 2: GS/DFT DRIVE: ON Unit 1A2: NAV SIM: 0	Same as 1 above	GS/DFT indicator dial nulls and SERVO FAULT indicator lamp is extinguished.
4	None	Unit 2: SERVO LOOP: DFT GS/DFT DRIVE. OFF Unit 1A2: NAV SIM 5R	Same as 1 above	GS/DFT indicator dial does not null and SERVO FAULT indicator lamp flashes.
5	None	Unit 2. gs/DFT DRIVE: ON Unit 1A2: NAV SIM 15R	Same as 1 above	GS/DFT indicator dial nulls and SERVO FAULT indicator lamp is extinguished.
6	None	Unit 1A2: NAV SIM. 0	Same as 1 above .	GS/DFT indicator dial nulls and SERVO FAULT indicator lamp is extinguished.
7	None	Unit 2: GS/DFT DRIVE: OFF	Same as 1 above	GS/DFT indicator dial remains at 0 and SERVO FAULT indicator lamp remains extinguished.
8	None	Unit 2: NAVIGATION· GS GS/DFT DRIVE: ON Unit 1A2· NAV SIM: 15L	Same as 1 above	GS/DFT indicator dial does not null and SERVO FAULT indicator lamp remains extinguished.
9	None	Unit 2. NAVIGATION· MANUAL	Same as 1 above .	GS/DFT indicator does not null and servo fault lamp remains extinguished.
10	None	Unit 2· SERVO LOOP. GS	Same as 1 above . .	GS/DFT indicator dial does not null and SERVO FAULT indicator lamp remains extinguished.
11	None	Unit 2. NAVIGATION GS	Same as 1 above .	GS/DFT indicator dial nulls and SERVO FAULT indicator lamp is extinguished.

b. Troubleshooting Procedure. The following troubleshooting procedure will aid in localizing a servo loop **trouble** symptom to defective servo amplifier 2A5 or to the remaining components of the servo loop. If the trouble is determined to be in the servo loop but not in the servoamplifier, a more detailed procedure is required to localize a specific synchro, control, or gear train. For this reason a supplementing test procedure (para 3-20) follows the troubleshooting table. This procedure is used when replacement of servoamplifier 2A5 does not remedy the trouble symptom. It is not intended to be used as a performance test of the servo loop. The simplified wiring diagram shown in figure FO-7 shows cables, wiring, components, and test points pertaining to the servo loop.

Table 3-10. Servo Loop Troubleshooting

Item No.	Trouble Symptom	Probable Trouble	Checks and Corrective Actions
1	GS/DFT indicator fails to null and SERVO FAULT light remains on with the following test set control settings: NAVIGATION. AUTO GS/DFT DRIVE: ON NAV SIM: 15R SERVO LOOP: Operate from GS to DFT position and return to DFT after 20 seconds.	*a.* Defective servo amplifier 2A5. *b.* Defective synchro, relay, stepping motor, or reduction gear of the servo loop (fig FO-7)	*a* Replace servoamplifier 2A5 (fig 3-10) *b* If GS/DFT indicator fails to null in either position (GS or DFT) of the SERVO LOOP switch, and replacement of servoamplifier 2A5 does not remedy the trouble symptom, perform the detailed servo test of para 3-20. Replace any defective component(s) and realign synchros 1A2B1 and 2B2 (para 3-41 through 3-43).

3-20. Servo Loop Supplementary Tests for Troubleshooting (fig. 3-1 and FO-7)

a. Test Equipment Required. Voltmeter, digital AN/GSM-64B and Oscilloscope AN/USM-281C.

b. Test Connections and Conditions.

(1) Set up the equipment as instructed in paragraph 3-15c.

(2) Operate the test set group controls to the following positions:

CONTROL	*POSITION*	*LOCATION*
NAV SIM	0	Unit 1A2
NAVIGATION	AUTO	Unit 2
SERVO LOOP	DFT	Unit 2
GS/DFT DRIVE	ON	Unit 2
POWER	ON	Unit 2

(All other test set group controls may be in any position)

c. Initial Test Equipment Calibration. None Required.

d. Procedure. The following procedure supplements the servo loop test of paragraph 3-19. This procedure will be used as an aid to troubleshooting the servo loop when replacement of servo amplifier 2A5 does not remedy the trouble symptoms, and is not intended to be used as a performance test of the servo loop. PROBABLE DEFECTIVE COMPONENTS ARE SHOWN IN PARENTHESES BELOW EACH STANDARD IN THE PERFORMANCE STANDARD COLUMN. The servo loop wiring diagram of figure FO-7 shows cables, wiring, components, and test points pertaining to the servo loop.

Table 3-11. Servo Loop Supplementary Test

Step No.	Control Settings: Test Equipment	Control Settings: Equipment Under Test	Test Procedure	Performance Standard
1	Digital voltmeter function; ac RANGE AUTO	None	*a.* Measure the voltage between test points 1A2J18-8 and 1A2J18-9 *b* Measure the voltage between test points 2J4-1 and 2J4-2	*a* 26 ± 2 vac (1A2T1, fig 3-7) or (1A2K1, fig 3-8) *b* 26 ± 2 vac (1A2T1, fig 3-7) or (1A2K1, fig 3-8)
2	Digital voltmeter. FUNCTION: DC	Unit 2 SERVO LOOP: GS	Measure the voltage between test points 1A2J11-61 and 1A2J11-49 (28 vdc return)	+0 7 ± 0 2 vdc (1A2Q1)
3	Oscilloscope VOLTS/DIV 2 TIME/DIV: 2ms	Unit 2. NAVIGATION: MANUAL SERVO LOOP DFT	*a.* Place the scope probes between test points 1A2J18-13 and 1A2J18-14	*a* 15 ± 2 vac (1A2B1, fig 3-8)
	VERT MODE: ADD NOTE Two oscilloscope probes required.	Unit 1A2: NAV SIM: 15R	*b* Manually vary the NAV SIM control on unit 1A2 throughout its range	*b* The oscilloscope indication shall be minimum when the NAV SIM control is at zero, and shall peak to 15 ± 2 vac at 15R and 15L (1A2B1, 1A2K5 or 1A2K6, fig 3-6 or 3-8)
4	None	None	Repeat *b* above with the oscilloscope probes between test points 2J4-17 and 2J4-18	Same as 3 above

Table 3-11. Servo Loop Supplementary Test - Continued

Step No.	Control Settings: Test Equipment	Control Settings: Equipment Under Test	Test Procedure	Performance Standard
5	. . . .	Unit 2: NAVIGATION: MANUAL SERVO LOOP: GS Unit 1A2: NAV SIM: 15R	*a.* Place the oscilloscope probes between test points 1A2J18-5 and 1A2J18-6. *b.* Manually vary the NAV SIM control throughout its range.	*a.* Same as 3 above. *b* The oscilloscope indication shall be minimum when the NAV SIM control is at zero, and shall peak to 15 ± 2 vac at 15R and 15L.
6	None	None	Repeat 5 above with the oscilloscope probes between test points 2J4-14 and 2J4-15.	Same as 5 above.
7	None	Unit 2: POWER OFF	Disconnect cable W4 from jack 1A2J18. Connect jumper cables and the digital voltmeter as shown in A, figure 3-1.	None
8	Digital voltmeter: FUNCTION. AC RANGE: AUTO	Unit 2· POWER ON SERVO LOOP: DFT Unit 1A2: ILLUM: ON	Operate the NAV SIM control on unit 1A2 to obtain maximum reading on the voltmeter.	NAV SIM control shall indicate 0 ± 4 divisions when the voltage meter reading is maximum.
9	None	Unit 2: POWER: OFF	Connect the equipment as shown in B, figure 3-1.	none
10	None	Unit 2: POWER: ON SERVO LOOP· DFT Unit 1A2: ILLUM: ON	Operate the NAV SIM control to obtain minimum reading on the voltmeter.	NAV SIM control shall indicate 0 ± 1 divisions
11	None	Unit 2 POWER: OFF	Disconnect jumper leads and the digital voltmeter, and reconnect cable W4 to jack 1A2J18 (fig FO-4).	None
12	Digital voltmeter: FUNCTION: K OHM	Unit 2. power; off	Disconnect cable W8 from jack 2J4 (fig FO-4).	None
13	None	None	Measure the following test points (fig FO-7) 2J4-8 to 2J4-9 (S1 to S2) 2J4-9 to 2J4-10 (S1 to S3) 2J4-8 to 2J4-10 (S2 to S3) 2J4-1 to 2J4-2 (R1 to R2)	Nominal resistance: 12 ohms 12 ohms 12 ohms 39 ohms (2B2, fig. 3-11).
14	None	None	Reconnect cable W8 to jack 2J4 (fig FO-4).	None

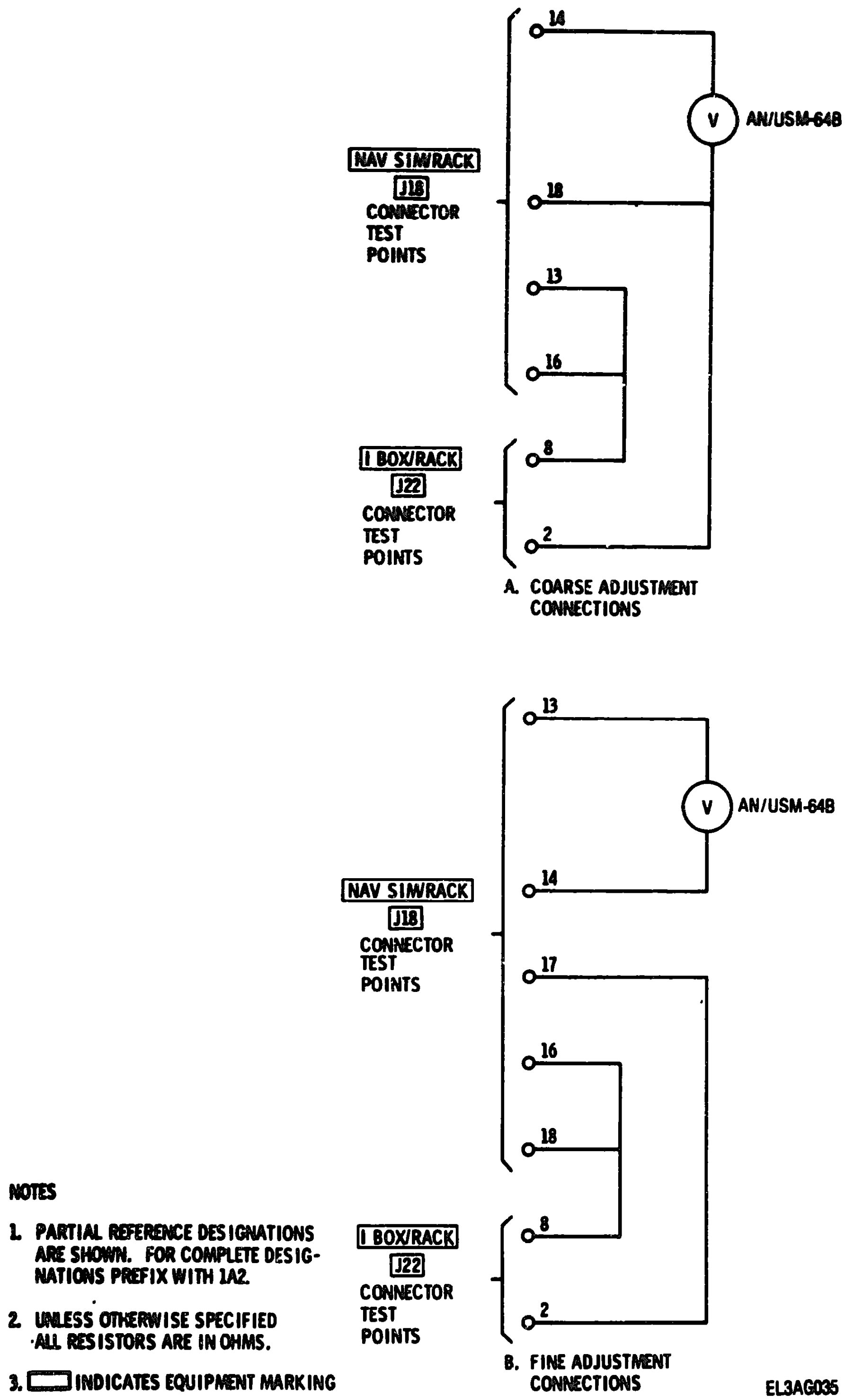


Figure 3-1. Control synchro adjustment test setup (A and B).

3-21. Clock Waveform Troubleshooting.

a. Bench Test. Perform the clock waveform bench test as described in table 3-12 below.

Table 3-12. Clock Waveform Test

Step No.	Control Settings: Test Equipment	Control Settings: Equipment Under Test	Test Procedure	Performance Standard
1	None	Unit 2: RANGE: 50 ANTENNA: RIGHT	Connect oscilloscope to test point 1A2J11-37 and observe waveform.	Waveform A, figure 3-2.
2	None	Unit 2: INTENSITY: Maximum DISPLAY: FT Unit 1A2: TEST VIDEO: ON FT GAIN: Variable	Connect oscilloscope to test point 1A2J1-2 and observe waveform.	Waveform B, figure 3-2.
3	None	Unit 2: INTENSITY: Minimum Unit 1A2: TEST VIDEO: OFF FT GAIN: Maximum VIDEO AMPLITUDE: Variable	Connect oscilloscope to test point 1A2J1-2 and observe waveform.	Waveform C, figure 3-2.
4	None	Unit 2: RANGE: 25	Connect oscilloscope to test point 2J1-45 and observe waveform.	Waveform D, figure 3-2.
5	None	Unit 2: RANGE: 50	Connect oscilloscope to test point 2J1-45 and observe waveform.	Waveform E, figure 3-2.
6	None	Unit 2: RANGE: 100	Connect oscilloscope to test point 2J1-45 and observe waveform.	Waveform F, figure 3-2.
7	Oscilloscope: Dc coupled	Unit 2: ANTENNA: RIGHT	Connect oscilloscope to test point 2J4-24 and measure displayed signal voltage.	+4.0 ± 0.5 vdc
8	None	Unit 2: ANTENNA: BOTH	Connect oscilloscope to test point 2J4-24 and observe waveform.	Waveform G, figure 3-2.
9	Oscilloscope: Dc coupled	Unit 2: ANTENNA: LEFT	Connect oscilloscope to test point 2J4-24 and measure displayed signal voltage	-4.0 ± 0.5 vdc
10	None	Unit 2: ANTENNA: BOTH	Connect oscilloscope to test point 1A2J11-32 and observe waveform.	Waveform H, figure 3-2.
11	Oscilloscope: Dc coupled	Unit 2: ANTENNA: RIGHT	Connect oscilloscope to test point 1A2J11-32 and measure displayed signal voltage.	+4.74 ± 0.25 vdc
12	None	Unit 2: ANTENNA. BOTH	Connect oscilloscope to test point 1A2J11-33 and observe waveform.	Waveform J, figure 3-2.
13	Oscilloscope: Dc coupled	Unit 2: ANTENNA: LEFT	Connect oscilloscope to test point 1A2J11-33 and measure displayed signal voltage.	+4.75 ± 0.25 vdc

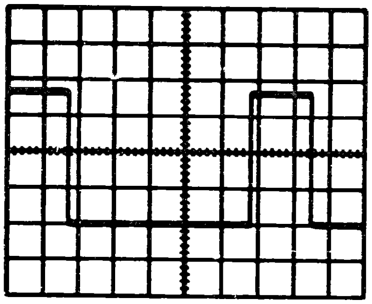
b. Troubleshooting Procedure. **The following troubleshooting procedure is referenced to the test set group waveforms A, B,** C, D, E, F, G, H, and J of **figure 3-2. The signals represented by these waveforms originate in either the 5-MHz oscillator** and prf counter lA2A1, antenna counter lA2A2 or video amplifier lA2A6. Use of the troubleshooting procedure will localize a clock waveform trouble to one of these three modules.

Table 3-13. Clock Waveform Troubleshooting

Item No.	Trouble Symptom	Probable Trouble	Checks and Corrective Actions
1	Waveform A (fig. 3-2), measured at test point 1A2J11-37, is abnormal.	Defective 5-MHz oscillator and prf counter 1A2A1	Replace 5-MHz oscillator and prf counter 1A2A1 (fig 3-7) **NOTE** If 1A2A1 is not at fault, refer to figure FO-15 and check all inputs to 1A2A1.
2	Waveform B (fig. 3-2), measured at test point 1A2J1-2, is abnormal with the test set group controls set to the following positions· **NOTE** Waveform B, at this point has an amplitude of approximately 3 volts peak-to-peak. Unit 2· INTENSITY. Minimum Unit 1A2· TEST VIDEO: ON FT GAIN: Maximum VIDEO AMPLITUDE. Variable	Defective video amplifier 1A2A6.	Replace video amplifier 1A2A6 (fig 3-5). **NOTE** If 1A2A6 is not at fault, refer to figure FO-20 and check all inputs to 1A2A6
3	Waveform C (fig. 3-2) measured at test point 1A2J1-2, is abnormal with the test set group controls set to the following positions: Unit 2: INTENSITY: Minimum Unit 1A2. TEST VIDEO: OFF FT GAIN: Maximum VIDEO AMPLITUDE: Variable	Same as 2 above.	Same as 2 above.
4	Waveform D (fig. 3-2), measured at test point 2J1-45, is abnormal with the test set group controls set to the following position: Unit 2: RANGE: 25	Same as 1 above.	Same as 1 above
5	Waveform E (fig. 3-2), measured at test point 2J1-45, is abnormal with the RANGE switch on unit 2 set to 50.	Same as 1 above.	Same as 1 above.
6	Waveform F (fig. 3-2) measured at test point 2J1-45, is abnormal with the RANGE switch on unit 2 set to 100.	Same as 5 above.	Same as 5 above.
7	A voltage of +4.0 to +4.5 vdc is not present at test point 2J4-24 with the ANTENNA switch on unit 2 set to RIGHT.	Defective antenna counter 1A2A2.	Replace antenna counter 1A2A2 (fig 3-7) **NOTE** If 1A2A2 is not at fault, refer to figure FO-16 and check all inputs to 1A2A2.
8	Waveform G (fig. 3-2), measured at test point 2J4-24, is abnormal with the ANTENNA switch on unit 2 set to BOTH.	Same as 7 above	Same as 7 above

Table 3-13. Clock Waveform, Troubleshooting - Continued

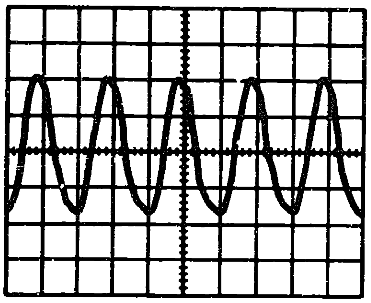
Item No.	Trouble Symptom	Probable Trouble	Checks and Corrective Actions
9	A voltage of -4.1 to -4.5 vdc is not present at test point 2J4-24 with the ANTENNA switch on unit 2 set to LEFT.	Same as 7 above.	Same as 7 above.
10	Waveform H (fig. 3-2), measured at test point 1A2J11-32, is abnormal with ANTENNA switch on unit 2 set to BOTH.	Same as 7 above.	Same as 7 above.
11	A voltage of +4.5 to +5.0 vdc is not present at test point 1A2J11-32 with the ANTENNA switch on unit 2 set to RIGHT.	Same as 7 above.	Same as 7 above.
12	Waveform J (fig. 3-2), measured at test point 1A2J11-33, is abnormal with ANTENNA switch on unit 2 set to BOTH.	Same as 7 above.	Same as 7 above.
13	A voltage of +4.5 to +5 0 vdc is not present at test point 1A2J11-33 with the ANTENNA switch on unit 2 set to LEFT	Same as 7 above.	Same as 7 above.



TEST POINT: 1A2J11-37

VOLTS/DIV: 1
TIME/DIV: .2 MSEC
SYNC: EXT

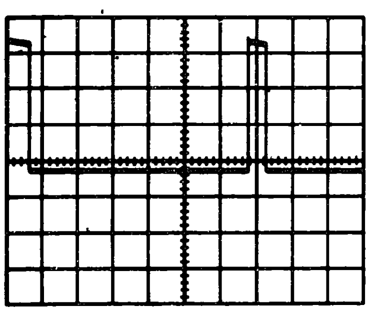
A. SWEEP GATE



TEST POINT: 1A2J1-2

VOLTS/DIV: 2
TIME/DIV: .1 µSEC
SYNC: EXT

B. TEST VIDEO

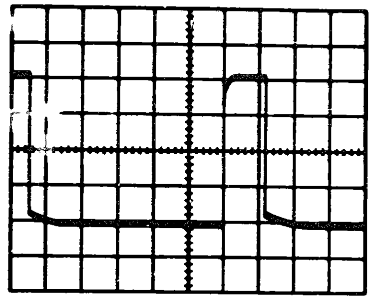


TEST POINT: 1A2J1-2

VOLTS/DIV: 2
TIME/DIV: .2 MSEC
SYNC: EXT

C. FT VIDEO

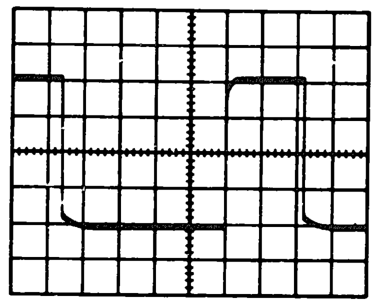
NOTE:
ALL WAVEFORMS TAKEN
WITHOUT PROBE.



TEST POINT: 2J1-45

VOLTS/DIV: 2
TIME/DIV: .2 MSEC
SYNC: EXT

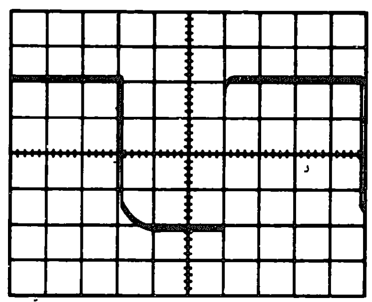
D YOKE CLAMP (25 km)



TEST POINT: 2J1-45

VOLTS/DIV: 2
TIME/DIV: .2 MSEC
SYNC: EXT

E. YOKE CLAMP (50 km)



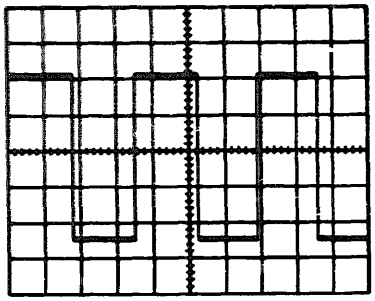
TEST POINT: 2J1-45

VOLTS/DIV: 2
TIME/DIV: .2 MSEC
SYNC: EXT

F. YOKE CLAMP (100 km)

EL3AG058

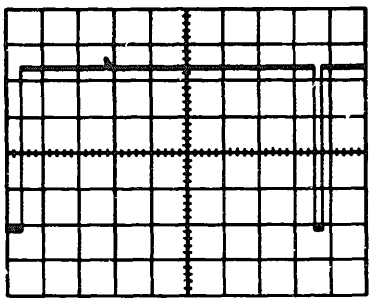
Figure 3-2. Test Set Group, Indicator, Radar OQ-63A/APS-94D, waveforms (sheet 1 of of *5)*



TEST POINT: 2J4-24

VOLTS/DIV: 2
TIME/DIV: 50 MSEC
SYNC: INT (+)

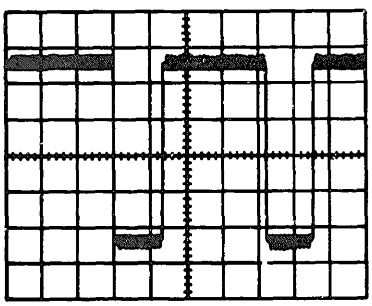
G. ANTENNA GATE



TEST POINT: 1A2J11-32

VOLTS/DIV: 2
TIME/DIV: 10 MSEC
SYNC: INT (-)

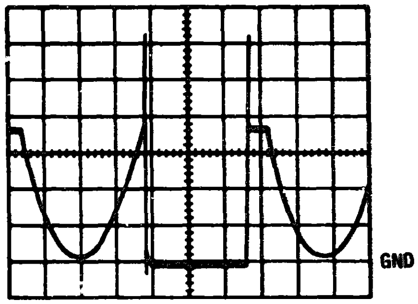
H. FT. ENABLE



TEST POINT: 1A2J11-33

VOLTS/DIV. 2
TIME/DIV: 20 MSEC
SYNC: INT(+)

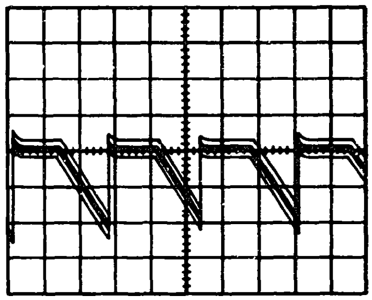
J. MT ENABLE



TEST POINT: 1A2J11-23

VOLTS/DIV: 2
TIME/DIV: 2 MSEC
SYNC· EXT

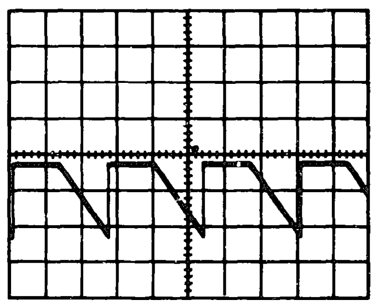
K. ASTIGMATISM



TEST POINT: 1A2J14-10

VOLTS/DIV: .5
TIME/DIV: .5 MSEC
SYNC: EXT

L. VERTICAL SWEEP (15 deg)



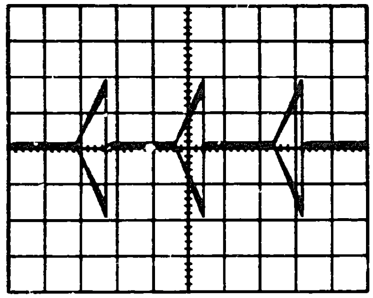
TEST POINT· VERTICAL SWEEP TEST JACK

VOLTS/DIV: .2
TIME/DIV: .5 MSEC
SYNC: EXT

M. VERTICAL SWEEP (1.8 deg)

EL3AG033

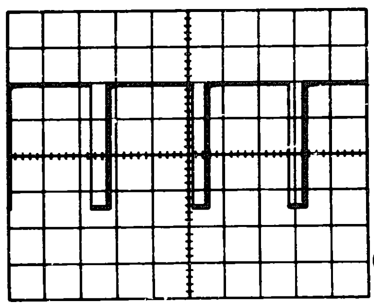
Figure 3-2. Test Set Group Indicator, Radar OQ-63A/APS-94D, waveforms (sheet 2 of 5).



TEST POINT 1A2J14-8

VOLTS/DIV 1
TIME/DIV .5 MSEC
SYNC. EXT

N HORIZONTAL SWEEP (50 km)



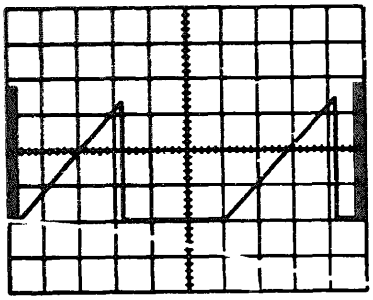
TEST POINT 1A2J1-5

/OLTS/DIV 20
TIME/DIV .5 MSEC
SYNC EXT

P UNBLANK

EL3AG034 3

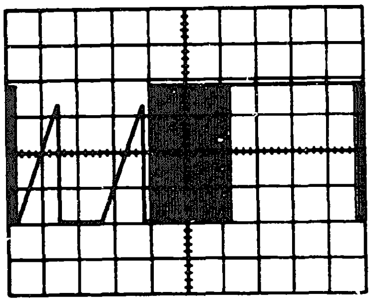
Figure 3-2. Test Set Group, Indicator, Radar OQ-63A/APS-94D, waveforms (sheet 3 of 5)



TEST POINT 1A1J7-1

VOLTS/DIV 10
TIME/DIV 2MS
SYNC EXT

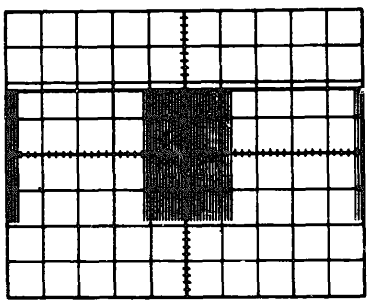
R ADAS RAMPS BCD MODE



TEST POINT 1A1J7-1

VOLTS/DIV 10
TIME/DIV 5 MS
SYNC EXT

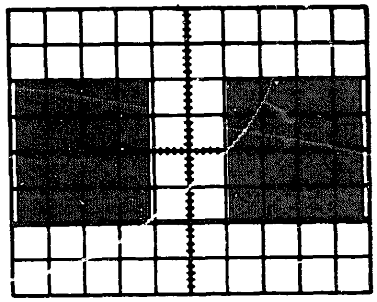
S ADAS RAMP ALT MODE



TEST POINT 1A1J7-1

VOLTS/DIV 10
TIME/DIV 5 MS
SYNC EXT

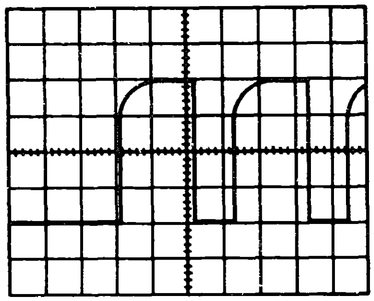
T ADAS RAMPS NUM MODE



TEST POINT 1A1J7-12

VOLTS/DIV 20
TIME/DIV 5MS
SYNC EXT

U UNBLANKING



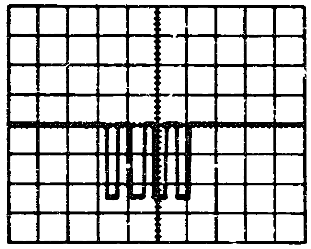
TEST POINT 1A1J7-12

VOLTS/DIV 20
TIME/DIV 10 μS
SYNC EXT

V UNBLANKING

EL3AG031

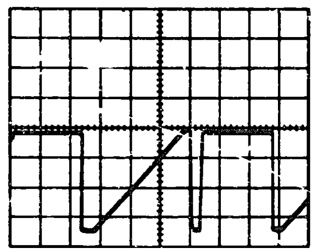
Figure 3-2. Test Set Group, Indicator, Radar OQ-63A/APS-94D, waveforms (sheet 4 of 5)



TEST POINT 1A1J10

VOLTS/DIV 1
TIME/DIV 200 μ SEC
SYNC EXT

W ECCM VIDEO



TEST POINT 1A1J11

VOLTS/DIV 1
TIME/DIV 200 μ SEC
SYNC EXT

X ECCM DEFLECTION

EL3AG050

Figure Radar OQ-63A/APS-94D, waveforms (sheet 5 of **5)**

3-22. Film Speed Troubleshooting

a. *Bench* Test. Perform the film speed bench test as described in table **3-14 below.**

Table 3-14 Film Speed Teat

Step No.	Control Settings		Test Procedure	Performance Standard
	Test Equipment	Equipment Under Test		
1	Oscilloscope: VOLTS/DIV: 5 TIME/DIV: 1 Sec	*a.* Unit 1A2. FILM SPEED CONTROL: Fully clockwise *b.* Unit 1A2: FILM SPEED CONTROL: Fully counterclockwise	*a.* Connect oscilloscope to test point 2J4−85 and measure signal voltage *b.* Connect oscilloscope to test point 2J4−85 and measure signal voltage.	*a.* +25.5 ±1 5 vdc *b* +5 0 ±1 0 vdc

Table 3-14. Film Speed Test - Continued

Step No.	Control Settings: Test Equipment	Control Settings: Equipment Under Test	Test Procedure	Performance Standard
2	Digital voltmeter: RANGE: AUTO FUNCTION: VAC	Unit 1A1: FILM SPEED: OFF	Connect digital voltmeter to test points 1A1J4–16 (+) and 1A1J4–17 (-) and adjust the input variable transformer for 115 vac reading on digital voltmeter.	115 ±0.02 vac
3		Unit 1A1: FILM SPEED: CAL	Connect digital voltmeter to test points 1A1J3–5 (+) and 1A1J3–6 (-) and measure signal voltage.	2.700 ±0.010 vac
4		Unit 1A1: FILM SPEED: LOW	Connect digital voltmeter to test points 1A1J3–5 (+) and 1A1J3–6 (-) and measure signal voltage.	0.81 to 0.84 vac
5		Unit 1A1 FILM SPEED: HIGH	Same as 4 above.	13.0 to 13.4 vac

b. Troubleshooting Procedure. The following procedure is used in troubleshooting the film speed voltages. Film speed voltage circuits are shown in figure FO–14 and will be an aid to maintenance personnel when troubleshooting.

Table 3-15. Film Speed Troubleshooting

Item No.	Trouble Symptom	Probable Trouble	Checks and Corrective Actions
1	With the oscilloscope connected to 2J4–85 dc level does not vary from +4 vdc to +27 vdc when the FILM SPEED CONTROL on unit 1A2 is varied from full ccw to full cw position.	*a.* Defective BITE circuit 1A2A4. *b.* Defective FILM SPEED control 1A2R18.	*a.* Replace BITE circuit 1A2A4 (fig. 3–7). If still defective proceed to *b* below. *b.* Replace FILM SPEED control 1A2R18 (fig. 3–7).
2	With the digital voltmeter connected to test point 1A1J3–5 with return referenced to test point 1A1J3–6, ac level does not go from zero to 13.4 volts when FILM SPEED switch is operated from OFF to CAL.	*a.* Defective transformer 1A1T1. *b* Defective resistor network on 1A1A2. *c* Defective FILM SPEED switch 1A1S3.	*a.* Check for presence of 196 vac between test points 1A1J1–1 and 1A1J1–2. If present check transformer 1A1T1 output. If not present, refer to the primary power distribution troubleshooting procedure (para 3–16) *b* Substitute +28 vdc power supply 1A1A2 (fig. 3–4). If still defective, proceed to *c* below. *c* Replace FILM SPEED switch 1A1S3.

3-23. Intensity Control Voltage Troubleshooting

a. Bench Test. Perform the intensity control voltage bench test as described in table 3-16 below.

Table 3-16. Intensity Control Voltage Test

Step No.	Control Settings		Test Procedure	Performance Standard
	Test Equipment	Equipment Under Test		
1	Oscilloscope: VOLTS/DIV: 5 TIME/DIV: 1 Sec	Unit 2: DISPLAY: FT INTENSITY: Minimum	*a.* Connect oscilloscope to test point 1A2J1-2 and observe voltage level as the INTENSITY control on unit 2 is increased to maximum. *b.* Operate the DISPLAY switch on unit 2 to MT position and observe voltage level displayed on oscilloscope.	*a.* Voltage level rises from -28 to 0 vdc as control is increased. *b* Voltage level drops rapidly to -27 ±1 vdc.
2	None	Unit 2: DISPLAY: MT INTENSITY: Minimum	*a.* Connect oscilloscope to test point 1A2J11-30 and observe voltage level as the INTENSITY control on unit 2 is increased to maximum. *b.* Operate the DISPLAY switch on unit 2 to MT position and observe voltage level displayed on oscilloscope.	*a.* Same as 1*a* above *b* Same as 1*b* above.

b. Troubleshooting Procedure. The following procedure is used to troubleshoot the intensity control voltage circuits. The intensity control voltage circuits are shown in FO-6 and will be used as an aid for maintenance personnel when troubleshooting.

Table 3-17. Intensity Control Voltage Troubleshooting

Item No.	Trouble Symptom	Probable Trouble	Checks and Corrective Actions
1	The dc voltage measured at test point 1A2J1-2 does not change from -28 to 0 vdc when the INTENSITY control on unit 2 is varied from minimum to maximum and the DISPLAY control on unit 2 is in the FT position	Defective video amplifier 1A2A6	Replace video amplifier 1A2A6 (fig 3-5).
2	With the DISPLAY control on unit 2 in the MT position, the voltage at test point 1A2J1-2 is not between -26 vdc and -28 vdc.	Same as 1 above.	Same as 1 above.
3	The dc voltage measured at test point 1A2J11-30 does not change from -28 to 0 vdc when the INTENSITY control on unit 2 is varied from minimum to maximum and the DISPLAY CONTROL on unit 2 is in the FT position.	Defective yoke simulator 2A1.	Replace yoke simulator 2A1 (fig 3-12)
4	With the DISPLAY control on unit 2 in the MT position, the voltage at test point 1A2J11-30 is not between -26 vdc and -28 vdc.	Same as 3 above	Same as 3 above

3-24. Vertical Sweep Waveform Troubleshooting

a. Bench Test. **Perform the vertical sweep waveform test as described in table 3–18 below.**

Table 3-18. Vertical Sweep Waveform Test

Step No.	Control Settings		Test Procedure	Performance Standard
	Test Equipment	Equipment Under Test		
1	None	Unit 1A2: VERTICAL OFFSET OVERRIDE: ON	*a.* Connect oscilloscope to test point 1A2J14–10 and observe waveform displayed, while adjusting VERTICAL AMPLIFIER SWEEP LENGTH and CENTER controls on unit 2.	*a.* Waveform L, figure 3–2.
		Unit 2: RANGE: 100 ANTENNA: LEFT DISPLAY: FT DRIFT ANGLE: 15 VERTICAL AMPLIFIER OPERATE TEST: OPERATE	*b.* Operate DISPLAY switch on unit 2 to MT position and observe voltage level on oscilloscope.	*b.* 0 ±0.3 vdc (noise may be present).
2	None	Unit 2: DISPLAY: FT DRIFT ANGLE: 1.8	Connect oscilloscope to vertical sweep test jack (VERTICAL AMPLIFIER section) on unit 2 and observe waveform while adjusting VERTICAL AMPLIFIER SWEEP LENGTH control on unit 2.	Waveform M, figure 3–2.
3	....	Unit 2: DISPLAY: MT DRIFT ANGLE· 15	*a.* Connect oscilloscope to test point 1A2J11–10 and observe waveform displayed while adjusting the VERTICAL AMPLIFIER SWEEP LENGTH control on unit 2.	*a.* Waveform L, figure 3--2.
			b Operate DISPLAY switch on unit 2 to FT position and observe the voltage level displayed on the oscilloscope connected to test point 1A2J11–10	*b* 0 ±0 3 vdc (noise may be present).

b. Troubleshooting Procedure. **The following troubleshooting procedure is referenced to the test set group waveforms L and M of figure 3–2. The signals represented by these waveforms originate in either video amplifier 1A2A6 or vertical amplifier 2A3. Use of the troubleshooting procedure will localize a vertical sweep trouble to one of these two modules.**

Table 3-19. *Vertical Sweep Waveform Troubleshooting*

Item No.	Trouble Symptom	Probable Trouble	Checks and Corrective Actions
1	Waveform L (fig. 3–2), measured at test points is abnormal with test set controls set as instructed in step 1 or 3 of paragraph 3–24*a*.	Defective video amplifier 1A2A6.	Replace video amplifier 1A2A6 (fig 3–5).

Table 3-19. Vertical Sweep Waveform Troubleshooting - Continued

Item No.	Trouble Symptom	Probable Trouble	Checks and Corrective Actions
2	Signal measured at test points is not 0 ±0.3 vdc with test set controls set as instructed in step 1 or 3 of paragraph 3–24a except, that DISPLAY control is changed from FT to MT.	Same as 1 above.	Same as 1 above.
3	Waveform M (fig. 3–2), measured at the vertical sweep test jack (above) left of OPERATE/TEST switch) on panel 2 is abnormal with the test set group controls on unit 2 set to the following positions: DISPLAY: FT DRIFT ANGLE: 1.8 RANGE: 100 OPERATE/TEST: OPERATE VERTICAL AMPLIFIER CENTER: adjust as required. VERTICAL AMPLIFIER SWEEP LENGTH: adjust as required.	Defective sweep generator 2A4.	Replace sweep generator 2A4 (fig. 3–10).
4	Unit 1A1: VERTICAL OFFSET OVERRIDE: ON Signal measured at test point 1A2J11–10 is not 0 ±0.3 vdc with the test set group controls set as in 3 above except that the DRIFT ANGEL control is changed from 1.8 to 15. NOTE Signal may be noisy.	Defective vertical amplifier 2A3.	Replace vertical amplifier 2A3 (fig. 3–12).
5	Waveform measured at test point 1A2J11–10 cannot be adjusted to the configuration of waveform L (fig. 3–2) by the VERTICAL AMPLIFIER SWEEP LENGTH and VERTICAL AMPLIFIER CENTER controls with the test set group controls positioned as in 3 above except that the DISPLAY control is changed from FT to MT position.	Same as 2 above.	Same as 2 above.

3-25. Horizontal Sweep Waveform Troubleshooting

a. *Bench Test.* Perform the horizontal sweep waveform bench test as described in table 3-20 below.

Table 3-20. Horizontal Sweep Waveform Test

Step No.	Control Settings		Test Procedure	Performance Standard
	Test Equipment	Equipment Under Test		
1	None	Unit 2: RANGE: 50 ANTENNA: BOTH DISPLAY: FT HORIZONTAL AMPLIFIER OPERATE-TEST: OPERATE	Connect the oscilloscope to test point 1A2J14-8 and observe waveform. Adjust the HORIZONTAL AMPLIFIER SWEEP LENGTH and CENTER controls and OFFSET GAIN control on unit 2.	Waveform N, figure 3-2.
2	None	Unit 2: DISPLAY: MT	Connect oscilloscope to test point 1A2J11-4 and observe waveform while adjusting HORIZONTAL SWEEP LENGTH control on unit 2.	Waveform N, figure 3-2.

b. Troubleshooting procedure. The following troubleshooting procedure is referenced to test set group waveform N of figure 3-2.

Table 3-21. Horizontal Sweep Waveform Troubleshooting

Item No.	Trouble Symptom	Probable Trouble	Checks and Corrective Actions
1	Waveform N, figure 3-2, measured at test point 1A2J14-8, is abnormal with test set group controls set as instructed in step 1 of paragraph 3-25*a*.	Defective horizontal amplifier 2A2.	Replace horizontal amplifier 2A2 (fig. 3-11).
2	Waveform N, figure 3-2, measured at test point 1A2J11-4, is abnormal with test set group controls set as in 1 above except DISPLAY control set to MT.	Same as 1 above.	Same as 1 above.
3	Similar to Waveform N, figure 3-2, but lesser in amplitude measured at horizontal sweep test jack (between CENTER and SWEEP LENGTH controls) on panel 2 is abnormal with the test set controls set as instructed in 1 of paragraph 3-25*a*.	*a.* Defective sweep generator 2A4. *b* Defective resistors 2TB3R16, potentiometer 2R3, switch 2S2 or capacitor 2TB3C1.	*a.* Replace sweep generator 2A4 (figure 3-10). *b.* Check and replace defective part (fig. 3-12 or 3-13).

3-26. Unblank Circuit Troubleshooting

a. Bench Test. **Perform the unblank circuits bench test as described in table 3-22 below.**

Table 3-22. Unblank Circuit Test

Step No.	Control Settings: Test Equipment	Control Settings: Equipment Under Test	Test Procedure	Performance Standard
1	None	Unit 1A2: UNBLANK ON Unit 2: RANGE: 25 ANTENNA: LEFT display; ft	Connect oscilloscope to test point 1A2J1-5 and observe waveform.	Waveform P, figure 3-2.
2	None	None	Operate the UNBLANK switch on unit 1A2 to OFF and observe the voltage level displayed on the oscilloscope.	+100 ±10 vdc

b. Troubleshooting Procedure. The following troubleshooting procedure is ***referenced*** to waveform P ***of*** figure 3-2.

Table 3-23. Unblank Circuit Troubleshooting

Item No.	Trouble Symptom	Probable Trouble	Checks and Corrective Actions
1	Waveform P of figure 3-2, measured at test point 1A2J1-5, is abnormal with the test set group controls set as follows: Unit 1A2: UNBLANK: ON Unit 2: RANGE: 25 ANTENNA: LEFT display; FT	Defective video amplifier 1A2A6.	Replace video amplifier 1A2A6 (fig. 3-5).
2	The voltage measured at test point 1A2J1-5 is not 100 ±10 vdc with the test set group controls positioned as in above except that the UNBLANK switch is positioned to OFF	Same as 1 above.	Same as 1 above.

3-27. Offset Circuit Troubleshooting

a. ***Bench*** *Test.* Perform the offset circuit bench test as described in table 3-24 below.

Table 3-24. Offset Circuit Test

Step No.	Control Settings: Test Equipment	Control Settings: Equipment Under Test	Standard	Performance
1	None	Unit 2: ANTENNA. BOTH RANGE. 100 DRIFT ANGLE: 15 DISPLAY: FT	Connect the oscilloscope to test point 1A2J1-8 and observe waveform.	Waveform N, figure 3-2

Table 3-24. Offset Circuit Test -Continued

Step No.	Control Settings: Test Equipment	Control Settings: Equipment Under Test	Test Procedure	Performance Standard
2	None	Unit 2: ANTENNA: RIGHT	*a.* Vary the LEFT HORIZONTAL OFFSET control on unit 2 and observe the waveform displayed on oscilloscope connected to to test point 1A2J1-8. *b.* Vary the RIGHT HORIZONTAL OFFSET control on unit 2 and observe that the ramp portion of the waveform offsets positive as control is increased.	*a.* Waveform is not affected as control is varied. *b.* Waveform offsets positive as control is increased.
3	None	Unit 2: ANTENNA: LEFT	*a.* Vary the RIGHT HORIZONTAL OFFSET control on unit 2 and observe the waveform displayed on oscilloscope connected to test point 1A2J1-8. *b.* Vary the LEFT HORIZONTAL OFFSET control on unit 2 and observe that the ramp portion of the waveform offsets negative as control is increased.	*a.* Waveform is not affected as control is varied. Waveform offsets negative as control is increased
4	None	Unit 1A2: VERTICAL OFFSET OVERRIDE: ON Unit 2: ANTENNA: LEFT RANGE: 100 VERTICAL AMPLIFIER OPERATE-TEST: OPERATE	*a.* Connect oscilloscope to test point 1A2J1-10 and observe waveform. *b.* Vary the VERTICAL OFFSET control on unit 2 and observe waveform.	*a.* Waveform L, figure 3-2. *b* Waveform is not affected as control is varied.
5	None	Unit 1A2: VERTICAL OFFSET OVERRIDE: OFF	Vary the VERTICAL OFFSET control clockwise on unit 2 and observe the waveform displayed on oscilloscope connected to test point 1A2J1-10.	Waveform moves in the negative direction as control is increased.

b. Troubleshooting Procedure. The following troubleshooting procedure is referenced to test set group waveforms N and L of figure 3-2.

Table 3-25. Offset Circuit Troubleshooting

Item No.	Trouble Symptom	Probable Trouble	Checks and Corrective Actions
1	Waveform N of figure 3-2, measured at test point 1A2J1-8, is abnormal with the test set group controls on unit 2 positioned as follows: ANTENNA: BOTH RANGE: 100 DRIFT ANGLE: 15 DISPLAY: FT OFFSET GAIN: Adjust as required.	*a.* Defective yoke simulator 2A1. *b* Defective offset control 2A7. *c* Defective resistors 2TB3R6, R38, R36, or potentiometer 2R11.	*a.* Replace yoke simulator 2A1 (fig. 3-12). *b.* Replace offset control 2A7 (fig. 3-12). *c* Check and replace defective part (fig. 3-12 and 3-13).

Table 3-25. Offset Circuit Troubleshooting - Continued

Item No.	Trouble Symptom	Probable Trouble	Checks and Corrective Actions
2	a. The sweep ramp of waveform N does offset as the LEFT HORIZONTAL OFFSET control is varied with the ANTENNA switch in the RIGHT position.	a. Defective switch 2S9.	a. Replace switch 2S9 (fig. 3-11).
	b. The sweep ramp of waveform N does not offset positive as the RIGHT HORIZONTAL OFFSET control on unit 2 is increased with the ANTENNA switch in the RIGHT position.	b. One or more of the following defective: (1) Offset control 2A7. (2) Resistors 2TB3R14, R13; potentiometer 2R12; switch 2S9; or transistor 2Q2 (right offset). (3) Resistors 2TB3R15, R35, R37, R10, R12, R8; potentiometer 2R5, 2R9; or transistor 2Q1 (left offset).	b. Replace one or more of the following: (1) Offset control 2A7 (fig. 3-12). (2) Check and replace defective part (fig. 3-11, 3-12, or 3-13). (3) Check and replace defective part (fig. 3-12 or 3-13).
3	a. The sweep ramp of waveform N does offset as the RIGHT HORIZONTAL OFFSET control is varied with the ANTENNA switch in the LEFT position.	a. Defective switch 2S9.	a. Replace switch 2S9 (fig. 3-11).
	b. The sweep ramp of waveform N does not offset negative as the LEFT HORIZONTAL OFFSET control on unit 2 is increased with the ANTENNA switch in the LEFT position.	b. One or more of the following defective: (1) Yoke simulator 2A1. (2) Offset control 2A7. (3) Offset amplifier 2A6.	b. Replace one or more of the following: (1) Yoke simulator 2A1 (fig. 3-12). If still abnormal, proceed to (2) below). (2) Offset control 2A7 (fig. 3-12). If still abnormal, proceed to (3) below. (3) Offset amplifier 2A6 (fig. 3-12).
4	Waveform L, measured at test point 1A2J1-10 is not movable in the negative (up) direction by the VERTICAL OFFSET control with the VERTICAL OFFSET OVERRIDE control in the OFF position.	a. Defective offset amplifier 2A6. b. Defective offset control 2A7 (fig. 3-12). c. Defective resistors 2TB3R11, R7, or potentiometer 2R10.	a. Replace offset amplifier 2A6 (fig. 3-12). If still abnormal, proceed to b below. b. Replace offset control 2A7 (fig. 3-12). c. Check and replace defective part (fig. 3-12 or 3-13).

3-28. Video Compression Troubleshooting

a Bench Test. Perform the video compression bench test as described in table 3-26 below.

Table 3-26. Video *Compression Test*

Step No.	Control Settings: Test Equipment	Control Settings: Equipment Under Test	Test Procedure	Performance Standard
1	None	Unit 1A2: FT GAIN: Maximum TEST VIDEO: OFF VIDEO AMPLITUDE: Maximum Unit 2: RANGE: 25 ANTENNA: RIGHT DISPLAY: FT INTENSITY: Maximum	a. Connect oscilloscope to test point 1A2J1-2 and observe waveform. b. Adjust VIDEO AMPLITUDE control on unit 1A2 for a peak voltage indication on the oscilloscope of 10 volts.	a. Waveform C, figure 3-2. b. Peak voltage of waveform is 10 volts.
2	None	Unit 2: ANTENNA: LEFT RANGE: 25	Observe peak voltage indicated on oscilloscope.	+10 ±0.5 volts peak

Table 3-26. Video Compression Test - Continued

Step No.	Control Settings		Test Procedure	Performance Standard
	Test Equipment	Equipment Under Test		
3	None	Unit 2: ANTENNA: BOTH RANGE: 100	Observe peak voltage level indicated on oscilloscope.	+4.2 ±0.4 volts peak
4	None	Unit 2: ANTENNA: RIGHT RANGE: 50	Observe peak voltage level indicated on oscilloscope.	+7.1 ±0.7 volts peak
5	None	Unit 2: ANTENNA: LEFT RANGE: 50	Observe peak voltage level indicated on oscilloscope.	+7.1 ±0.7 volts peak
6	None	Unit 2: ANTENNA: BOTH RANGE: 25	Observe peak voltage level indicated on oscilloscope.	+7.1 ±0.7 volts peak
7	None	Unit 2: ANTENNA: RIGHT RANGE: 100	Observe peak voltage level indicated on oscilloscope.	+4.2 ±0.4 volts peak
8	None	Unit 2: ANTENNA: LEFT RANGE: 100	Observe peak voltage level indicated on oscilloscope.	+4.2 ±0.4 volts peak
9	None	Unit 2: ANTENNA: BOTH RANGE: 50	Observe peak voltage level indicated on oscilloscope.	+4.2 ±0.4 volts peak

b. Troubleshooting Procedure. The following procedure is referenced to waveform C of figure 3–2.

Table 3-27. Video Compression Troubleshooting

Item No.	Trouble Symptom	Probable Trouble	Checks and Corrective Actions
1	Waveform C of figure 3–2, measured at test point 1A2J1–2, is abnormal or cannot be set to a minimum of 10 volts peak by adjustment of the VIDEO AMPLITUDE control.	Defective video amplifier 1A2A6.	Replace video amplifier 1A2A6 (fig. 3–5).
2	Waveform C of figure 3–2 is not 10 ±0.5 volts peak with the ANTENNA switch in the LEFT position and the RANGE switch set to 25.	Same as 1 above.	Same as 1 above.
3	Waveform C of figure 3–2 is not +4.2 ±0.4 volts peak with the test set group controls in the following position: ANTENNA: BOTH RANGE. 100	Same as 1 above	Same as 1 above.

Table 3-27. Video Compression Troubleshooting - Continued

Item No.	Trouble Symptom	Probable Trouble	Checks and Corrective Actions
4	Waveform C of figure 3-2 is not +7.1 ±0.7 volts peak with the test set group controls in the following positions: ANTENNA: RIGHT, LEFT or BOTH RANGE: 50 or 25	Same as 1 above.	Same as 1 above
5	Waveform C of figure 3-2 is not +4.2 ±0.4 volts peak with the test set group controls in any of the following positions: ANTENNA: RIGHT, LEFT or BOTH RANGE: 100 or 50	Same as 1 above	Same as 1 above

3-29. BITE, Sweep, Indicator **and Servo Fault Circuits Troubleshooting.**

a. Bench Test. Perform the BITE, sweep, indicator and servo fault circuit test as described in table 3-28 below.

Table 3-28. BITE. Sweep, Indicator and Servo Fault Circuits Test

Step No.	Control Settings		Test Procedure	Performance Standard
	Test Equipment	Equipment Under Test		
1	Digital voltmeter: RANGE: AUTO FUNCTION: VDC	None	*a.* Measure voltage level between test points 2J4-62 (+) and 2J4-23 (-). *b* Measure voltage level between test point 2J4-63 (+) and 2J4-23 (−). *c* Measure voltage level between test points 2J4-60 (+) and 2J4-23 (-) *d.* Measure voltage level between test points 2J4-29 (+) and chassis ground. *e.* Measure voltage level between test points 2J4-67 (+) and chassis ground. *f.* Measure voltage level between test points 2J4-25 (+) and chassis ground. *g* Measure voltage level between test point 2J4-69 (+) and chassis ground. *h* Measure voltage level between test points 2J4-70 (+) and chassis ground.	*a* +28 ±2 0 vdc *b* +28 ±2 0 vdc *c* +28 ±2 0 vdc *d* +19 5 ±0.5 vdc *e* +19.5 ±0 5 vdc *f* +19 5 ±0 5 vdc *g.* +19 5 ±0.5 vdc *h* +19 5 ±0 5 vdc
2	None	Unit 2: NAVIGATION· AUTO GS/DFT DRIVE· OFF Unit 1A2: NAV SIM: Same reading as GS/DFT indicated on Unit 2.	*a.* Observe SERVO FAULT indicator lamp on unit 2 *b* Operate NAV SIM control on Unit 1A2 to ±5 percent of GS/DFT reading	*a.* SERVO FAULT lamp is OFF *b* SERVO FAULT lamp flashes when NAV SIM control is moved greater than ±5 percent of the GS/DFT reading

Table 3-28. BITE, Sweep, Indicator and Servo Fault Circuits Test - Continued

Step No.	Control Settings: Test Equipment	Control Settings: Equipment Under Test	Test Procedure	Performance Standard
3	....	Unit 2: ANTENNA: BOTH	Observe SWEEP FAULT indicator lamp on unit 2.	Indicator lamp is off.
4	None	None	*a.* Disconnect one end of cable W21 connected between jacks 1A2J8 and 1A2J9 and observe SWEEP FAULT indicator lamp on unit 2 *b.* Connect cable end of W21 that was removed.	*a.* Indicator lamp flashes. *b* None.
5	None	Unit 2: DRIFT ANGLE 15 DISPLAY FT ANTENNA. LEFT Unit 1A2: UNBLANK: ON FT GAIN: Maximum VIDEO AMPLITUDE Maximum	*a* Operate the BITE switch on unit 1A2 to ON and observe FAILURE indicator lamp on unit 1A2. *b* Operate the ANTENNA switch on unit 2 to RIGHT and observe FAILURE indicator lamp on unit 2. *c* Operate the FT GAIN and VIDEO AMPLITUDE controls on unit 1A2, one at a time, to their minimum positions and observe the FAILURE indicator lamp on unit 1A2.	*a* FAILURE indicator lamp is off. *b* Same as *a* above. *c* FAILURE indicator lamp lights as each control is set to minimum position

b. Troubleshooting Procedure. The following procedure is to be used when the SWEEP, INDICATOR or SERVO FAULT lamps fail to light when failures are known to exist in the sweep, indicator, or servo circuits, or when failures are intentionally simulated.

Table 3-29. BITE, Sweep, Indicator and Servo Fault Circuits Troubleshooting

Item No.	Trouble Symptom	Probable Trouble	Checks and Corrective Actions
1	No +28 vdc (nominal) at any of the following test points: 2J4-62 2J4-63 2J4-60	Defective wiring or improper cable connections	Check wiring. Refer to wiring lists (para 3-51, 3-52, and 3-53) or figure FO-4
2	No +28 vdc (nominal) at test point 2J4-62; other test points in 1 above normal and no FAULT indication	Defective diode 1A2TB3CR2	Replace diode 1A2TB3CR2 (fig 3-9)
3	No +28 vdc (nominal) at test point 2J4-63; other test points in 1 above normal and no FAULT indication	Defective diode 1A2TB3CR3	Replace diode 1A2TB3CR3 (fig 3-9)
4	No +28 vdc (nominal) at test point 2J4-60; other test points in 1 above normal and no FAULT indication.	Defective diode 1A2TB3CR4	Replace diode 1A2TB3CR4 (fig 3-9)

Table BITE, Sweep, Indicator and Servo Fault Circuits Troubleshooting - Continued

Item No.	Trouble Symptom	Probable Trouble	Checks and Corrective Actions
5	No +20 vdc (nominal) at any of the following test points: 2J4-67 2J4-25 2J4-70 2J4-69 2J4-29	*a.* Defective wiring or improper cable connections. *b.* Defective low voltage power supply and regulator 1A2A3.	*a.* Refer to wiring lists paras 3-51, 3-52, and 3-53 or figure FO-4 *b.* Replace low voltage power supply and regulator 1A2A3 (fig. 3-7).
6	No +20 vdc (nominal) at test point 2J4-67; other test points in 5 above normal and no FAULT indication.	Defective diode 1A2TB3CR5.	Replace diode 1A2TB3CR5 (fig 3-9)
7	No +20 vdc (nominal) at test point 2J4-25 and 2J4-29; other test points in 5 above normal and no FAULT indication	Defective diode 1A2TB3CR6.	Replace diode 1A2TB3CR6 (fig 3-9)
8	No +20 vdc (nominal) at test point 2J4-70; other test points in 5 above normal and no FAULT indication	Defective diode 1A2TB3CR7	Replace diode 1A2TB3CR7 (fig 3-9).
9	No +20 vdc (nominal) at test point 2J4-69; other test points in 5 above normal and no FAULT indication.	Defective diode 1A2TB3CR8.	Replace diode 1A2TB3CR8 (fig 3-9)
10	SERVO FAULT indicator is not illuminated when the following actions are taken. Unit 2. NAVIGATION switch. AUTO GS/DFT DRIVE switch. OFF Unit 1A2: NAV SIM control manually set to ±5 divisions greater than GS/DFT indicator.	*a* Defective wiring or improper cable connections *b* Defective offset control 2A7 *c* Defective FAULT circuit 2A1	*a* Refer to wiring lists paras 3-51, 3-52, and 3-53 or figure FO-4 *b* Replace offset control 2A7 (fig 3-12) *c* Replace FAULT circuit 2A1 (fig 3-12)
11	SWEEP FAULT indicator is not illuminated when the following actions are taken· *a.* Remove W21 between 1A2J8 and 1A2J9. *b* Place the ANTENNA switch to BOTH *c.* Place the DISPLAY switch to FT.	*a.* Defective wiring or improper cable connections *b* Defective offset control 2A7 *c* Defective FAULT circuit 2A1	*a.* Refer to wiring lists (paras 3-51, 3-52, and 3-53) or figure FO-4. *b* Replace offset control 2A7 (fig. 3-12) *c* Replace FAULT circuit 2A1 (fig. 3-12)
12	FAILURE indicator lamp is on.	*a.* Defective or abnormal horizontal sweep circuit. *b* Defective or abnormal vertical sweep circuit *c* Defective or abnormal unblank circuit *d* Defective or abnormal video circuit *e* Defective BITE circuit 1A2A4	*a.* Refer to paragraph 3-25 *b* Refer to paragraph 3-24 *c* Refer to paragraph 3-26 *d* Refer to paragraph 3-28. *e* Replace BITE circuit 1A2A4 (fig 3-7)

3-30. ADAS Simulator Troubleshooting

a. Bench Test. Perform the ADAS simulator bench test as described in table 3–30 below.

Table 3-30. ADAS Simulator Test

Step No.	Control Settings		Test Procedure	Performance Standard
	Test Equipment	Equipment Under Test		
1	Pulse generator Pulse width: 1ms 15v Pulse frequency 33 pps (≈30ms) Oscilloscope TIME/DIV: 2 ms Sync scope on pulse generator	Unit 1A1 ADAS MODE BCD	Connect pulse generator to 1A1J9–1. Connect oscilloscope to test point 1A1J7–1 and observe waveform.	Waveform R, figure 3–2.
2	Oscilloscope TIME/DIV· 5ms	Unit 1A1 ADAS MODE ALT	Same as step 1 above	Waveform S, figure 3–2.
3	. . . .	Unit 1A1 ADAS MODE NUM	Same as step 1 above	Waveform T, figure 3–2.
4	Oscilloscope VOLTS/DIV: 20V	. . . .	Connect oscilloscope to test point 1A1J7–12 and observe waveform	Waveform U, figure 3–2
5	Oscilloscope TIME/DIV· 10us		Same as step 4 above	Waveform V, figure 3–2.

b. Troubleshooting Procedure. The following troubleshooting procedure is referenced to the test set group waveforms R, S, T, U, and V of figure 3–2. The signals represented by these waveforms originate in ADAS simulator 1A1A1.

Table 3-31. ADAS Simulator Troubleshooting

Item No.	Trouble Symptom	Probable Trouble	Checks and Corrective Actions
1	Waveform R of figure 3–2 measured at test point 1A1J7–1 is abnormal with ADAS MODE switch 1A1S1 set at BCD.	*a.* Defective ADAS simulator 1A1A1. *b* Defective ADAS MODE switch 1A1S1	*a.* Replace ADAS simulator 1A1A1 (fig. 3–4). If still defective, proceed to *b* below. *b.* Check and replace defective switch.
2	Waveform S of figure 3–2, measured at test point 1A1J7–1 is abnormal with ADAS MODE switch 1A1S1 set at ALT.	Same as 1 above.	Same as 1 above.
3	Waveform T of figure 3–2, measured at test point 1A1J7–1 is abnormal with ADAS MODE switch 1A1S1 set at NUM.	Same as 1 above.	Same as 1 above.
4	Waveform U of figure 3–2, measured at test point A1J7–12 is abnormal.	Defective ADAS simulator 1A1A1.	Replace ADAS simulator 1A1A1 (fig. 3–4).
5	Waveform V of figure 3–2, measured at test point 1A1J7–12 is abnormal.	Same as 4 above	Same as 4 above.

3-31. Monitor Adapter Input Simulator Troubleshooting

a. *Bench **Test.*** Perform the monitor adapter input simulator test as described in table 3-32 below

Table 3-32 . Monitor Adapter Input Simulator Test

Step No.	Control Settings		Test Procedure	Performance Standard
	Test Equipment	Equipment Under Test		
1	Oscilloscope VOLTS/DIV· 2V TIME/DIV· 200 us. Sync scope on connector J11 negative NOTE Connect 100-ohm termination (HP10100) to oscilloscope probe.	Unit 1A1.	Connect oscilloscope to 1A1J10 and observe waveform.	Waveform W, figure 3–2.
?	Same as step 1 above.	Unit 1A1	Connect oscilloscope to 1A1J11 and observe waveform	Waveform X, figure 3 -2

b. Troubleshooting Procedure. The following troubleshooting procedure is referenced to the test set group waveforms W and X cf figure 3–2. The signals represented by these waveforms originate in the monitor adapter input simulator 1A1A7.

Table 3-33. Monitor Adapter Input Simulator Troubleshooting

Item No.	Trouble Symptom	Probable Trouble	Checks and Corrective Actions
1	Waveform W of figure 3–2, measured at connector J10 is abnormal	Defective monitor adapter input simulator 1A1A7.	Replace monitor adapter input simulator 1A1A7
2	Waveform X of figure 3–2, measured at connector J11 is abnormal	Same as 1 above	Same as 1 above

3-32. **Dynamic Focus Troubleshooting**

a. Bench Test. Perform the dynamic focus bench test as described in table 3-34 below.

Table 3-34. Dynamic Focus Test

Step No	Control Settings		Test Procedure	Performance Standard
	Test Equipment	Equipment Under Test		
1	Oscilloscope (dc coupled). VOLTS/DIV 2 TIME/DIV· 0 2 MSEC SYNC: EXT	Unit 2· ANTENNA LEFT RANGE. 50 DRIFT ANGLE 15 degrees	Connect oscilloscope to test point 1A2J11–23 and observe waveform while adjusting LEFT HORIZONTAL OFFSET, VERTICAL OFFSET, and GAIN OFFSET, on Unit 2	Waveform K, figure 3–2

b. Troubleshooting Procedure The following troubleshooting procedure is used in troubleshooting the dynamic focus circuit.

Table 3-35. Dynamic Focus Troubleshooting

Item No.	Trouble Symptom	Probable Trouble	Checks and Corrective Action
1	Waveform K (fig. 3-1) measured at test point 1A2J11-23 is abnormal.	*a.* Defective wiring or improper cable connections.	*a.* Check wiring. Refer to wiring lists (para 3-51, 3-52, and 3-53) or figure FO-4.
		b. Defective sweep generator 2A4.	*b.* Replace sweep generator 2A4 (fig. 3-10).

3-33. High Voltage Load Troubleshooting

a. Bench Test. Perform the high voltage load bench test as described in table 3-36 below

WARNING

Dangerous voltages exist in the high voltage load circuits. Use extreme care when performing the following bench test.

Table 3-36. High Voltage Load Test

Step No.	Control Settings		Test Procedure	Performance Standard
	Test Equipment	Equipment Under Test		
1	Signal Generator SG-1105/G (pulse generator): Output amplitude: 1 volt. Pulse width: 300 microseconds. Frequency: 750 pps	Unit 1A1 (high voltage loads).	*a.* Remove 18 screws from the front panel of Unit 1A1.	*a.* None.
			b. Remove panel 1A1 from the cabinet.	*b.* None.
			c. Place the +28 VDC power supply high voltage loads 1A1A2 on an extender.	*c.* None.
			d. Connect pulse generator and one channel of oscilloscope to pin XA2-3 (signal) and E16 (ground) of +28 VDC power supply (fig. 3-4). Connect other oscilloscope channel to ANODE VOLTAGE 1V/10 KV terminal E3 on Unit 1A1.	*d.* Pulse generator displayed on both oscilloscope channels.
2	Same as 1 above	Same as 1 above.	Compare the amplitudes of the two oscilloscope channels.	Both channels should be the same amplitude.
3	Same as 1 above	Same as 1 above.	Check for ground dc offset of oscilloscope channel connected to ANODE VOLTAGE 1 V/10 KV terminal E3.	Ground offset should be less than ±0.5 vdc
4	Pulse generator: Output amplitude: 3 volts. Pulse width 300 microseconds Frequency: 750 pps.	Same as 1 above	Connect pulse generator and one channel of oscilloscope to pin XA2-C (signal) and E16 (ground) of +28 VDC PS high voltage loads 1A1A2 (fig. 3-4).	Pulse generator waveform displayed on both oscilloscope channels.
5	Same as 4 above	Same as 1 above	Connect the other oscilloscope channel to FOCUS VOLTAGE 2.75 V/2.75 KV terminal Z4 on Unit 1A1 Compare the amplitudes of the two channels of the oscilloscope.	Both channels should be the same amplitude

Table 3-36. High Voltage Load Test - Continued

Step No.	Control Settings		Test Procedure	Performance Standard
	Test Equipment	Equipment Under Test		
6	Same as 4 above.	Same as 1 above.	Check for ground dc offset of the oscilloscope channel connected to FOCUS VOLTAGE 2.75 V/2.75 KV terminal E4.	Offset should be less than ±0.5 vdc.
7	Same as 4 above.	Same as 1 above.	*a.* Remove card 1A1A2 from the extender and replace back in panel 1A1. *b.* Replace panel 1A1 back in cabinet. *c.* Replace 18 screws on the front panel of 1A1.	*a.* None. *b.* None. *c.* None.

b. Troubleshooting Procedure. The following procedure is used in troubleshooting the high voltage load circuits.

Table 3-37. High Voltage Load Troubleshooting

Item No.	Trouble Symptom	Probable Trouble	Checks and Corrective Actions
1	Waveform abnormal or missing at ANODE VOLTAGE 1V/10KV terminal E3 test point.	Defective +28 vdc power supply and high voltage load 1A1A2.	Replace +28 vdc power supply and high voltage load 1A1A2.
2	Waveform abnormal or missing at FOCUS VOLTAGE 2.75V/2.75KV terminal E4 test point.	Defective +28 vdc power supply and high voltage load 1A1A2.	Replace +28 vdc power supply and high voltage load 1A1A2.
3	*a.* Resistance from 1A1A6–E4 to ground 1A1A6–E5 with 1A1A2 removed is not 200K. *b.* Resistance from 1A1A6–E1 to 1A1A6–E5 not 1 meg ohm.	*a.* Defective anode load 1A1A6. *b.* Defective anode load 1A1A6.	*a.* Replace anode load 1A1A6. *b.* Replace anode load 1A1A6.
4	*a.* Resistance from 1A1A5–E4 to ground 1A1A5–E5 with 1A1A2 removed is not 110K ohm. *b.* Resistance from 1A1A5–E1 to 1A1A5–E5 not 1 megohm.	*a.* Defective focus load 1A1A5. *b.* Defective focus load 1A1A5.	*a.* Replace focus load 1A1A5 (fig. 3–4). *b.* Replace focus load 1A1A5 (fig. 3–4).

Section III. DIRECT SUPPORT MAINTENANCE OF TEST SET GROUP

3-34. General

a. Direct support maintenance of the test set group includes the following:

(1) Removal and replacement procedures.
(2) Cable Repair.
(3) Cleaning.
(4) Painting.
(5) Calibration.
(6) Physical tests and inspection.
(7) Electrical tests.

b. The above maintenance procedures supplement those maintenance procedures performed at the lower categories of maintenance. Refer to TM 11-3325-12 when servicing the equipment. performing operational checks, or preparing the equipment for shipment or limited storage.

3-35. Removal and Replacement Techniques

Most parts of the test set group can be reached and replaced without special procedures. The general directions given in *a* through *d* below apply.

a. Disassemble the equipment only to the extent needed to clean, adjust, repair or replace a part.

b. When performing maintenance, inspect the equipment for frayed or broken wiring, burns, arcing, missing or damaged piece parts, or other obvious signs of damage.

c. When replacing parts, note the position of the part and its leads. Replace parts in essentially the same position to avoid undesired coupling or shorting of wires.

d. Check the entire equipment for evidence of fungus, rust, and corrosion.

3-36. Removal and Replacement Procedures

WARNING

Remove all power from the equipment when performing removal and replacement procedures.

Removal and replacement of components at the direct support maintenance category are obvious upon inspection of the parts location illustrations and require no special instructions.

a. Test Set Subassembly MX–8638A/APS–94D, Unit 1A1.

(1) Remove the 18 screws securing unit 1A1 front panel to the case.

(2) Carefully lift the panel from the case.

(3) Refer to figures 3-3 and 3-4 for location of parts.

CAUTION

When removing plug-in modules from the chassis, pull straight out. Do not twist or otherwise put stress on these boards.

b. Test Set Subassembly MX–8638A/APS–94D, Unit 1A2.

(1) Remove the 18 screws securing unit 1A2 front panel to the case.

(2) Carefully lift the panel from the case.

(3) Refer to figure 3-5 through 3-9 for location of parts.

c. Test Set Subassembly MX–8639A/APS–94D, Unit 2.

(1) Remove the 18 screws securing unit 2 front panel to the case.

(2) Carefully lift the panel from the case.

(3) Refer to figure 3-10 through 3-13 for location of parts.

3-37. Cable Repair

NOTE

The wires within each cable are connected to associated pins as follows: pin A to pin A, pin B to pin B, etc. In certain cables, the wires are connected to associated pins as follows: pin A to 1, pin B to 2, etc.

a. Using ohmeter, check continuity of the cable from pin-to-pin.

b. Replace any wire indicating an open condition (no continuity).

c. Replace wire with wire of identical type, size, and gauge.

d. Cables which cannot be repaired by any of the above methods, refer to higher category of maintenance.

3-38. Cleaning

WARNING

The fumes of TRICHLOROETHANE are toxic. Provide thorough ventilation whenever it is used; avoid prolonged or repeated breathing of vapor. Do not use near an open flame or hot surface, trichloroethane is nonflammable but heat converts the fumes to a highly toxic phosgene gas the inhalation of which could result in serious injury or death. Prolonged or repeated skin contact with trichloroethane can cause skin inflammation. When necessary, use gloves, sleeves, and aprons which the solvent cannot penetrate.

a. Clean dirt and grime from switch contacts, cable connectors, and corroded terminal connections using clean cloth dampened (not wet) with trichloroethane.

b. Remove dirt and dust from interior and exterior surfaces of the equipment. Use clean cloth dampened with mild soap or detergent if necessary.

3-39. Painting

a. Minor damage to finishes on the equipment, such as small scratches, require touchup painting the affected areas only. Major surface damage requires complete repainting. Major surface damage to the equipment would normally be forwarded to higher category of maintenance.

b. Inspect the equipment to determine the extent of painting required. Refer to TB 43-0118, Field Instructions for Painting and Preserving Electronics Command Equipment, for information on painting.

3-40. Calibration

Paragraphs 3–41 through 3–43 contain the adjustment procedures necessary to calibrate the test

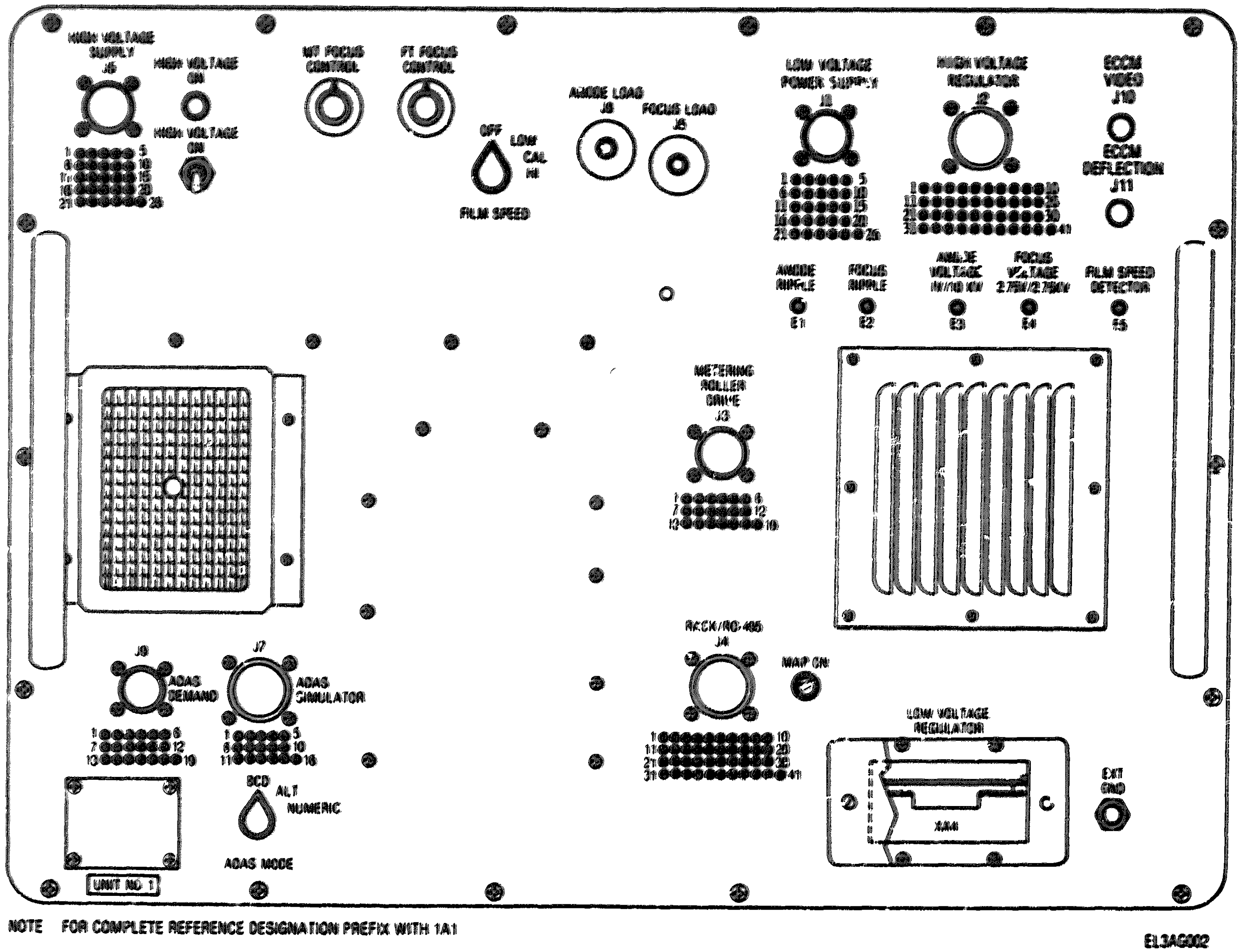


Figure 3-3. Test Set Subassembly MX-3433A/APS-94D, Unit 1A1 front panel, parts location.

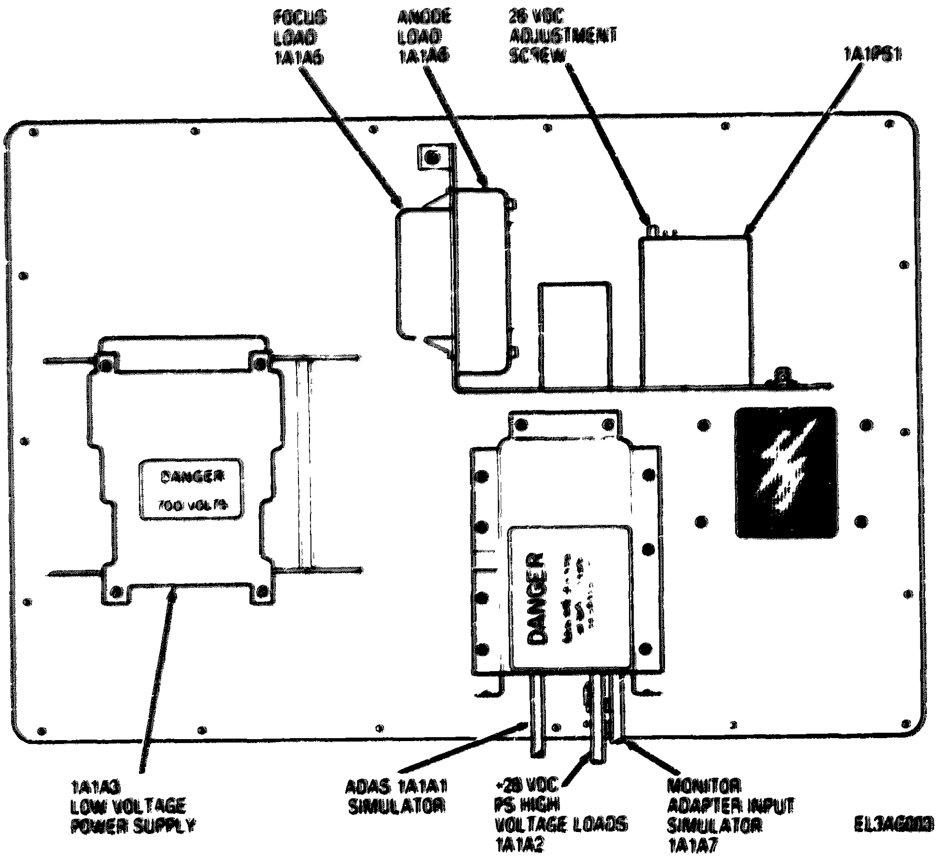


Figure 3-4. Test Set Subassembly MX-8638A/APS-94D, 1A1, rear chassis view, parts location.

set group. The only calibration required at the direct support maintenance level are the servo control synchro coarse and fine calibration, and GS/DFT dial calibration.

3-41. ServoControl-Synchro Coarse Calibration

a. Test Equipment Required. The multimeter is the only test equipment required for the calibration procedure.

b. Preliminary Procedures.

(1) Remove the 18 machine screws that secure panel of unit 1A2 in case.

(2) Carefully lift panel from case.

(3) Position all subassemolies on a clean workbench with a convenient access to both front and rear panel of unit 1A2.

(4) Deenergize 115 vac, 400 Hz and +28 vdc bench power circuits.

(5) Open (trip) AC, DC, LOW VOLTAGE, and HIGH VOLTAGE RESET circuit breakers on unit 1A2.

(6) Set POWER switch on unit 2 to OFF.

c. Test Setup and Conditions.

(1) Connect the equipment as illustrated in figure FO-4.

(2) Set all switches and controls to the off, down, or fully counterclockwise position.

d. Initial Test Equipment Calibration. Set the multimeter FUNCTION switch to AC VOLTS and connect the probes on the multimeter to measure 10 vac.

e. Calibration Procedure.

(1) Disconnect cable W4 from NAV SIM/RACK connector 1A2J18.

(2) Perform the equipment connections as illustrated in A, figure 3-1.

(3) Energize the 115 vac, 400 Hz and +28 vdc bench power circuits.

(4) Close all circuit breakers, except HIGH VOLTAGE RESET breaker on unit 1A2 and set the POWER switch on unit 2 to ON position.

(5) Turn the SERVO LOOP switch on unit 2 to DFT and set the ILLUM switch on unit 1A2 to ON.

(6) Disassemble the locking mechanism of the NAV SIM dial on the panel of unit 1A2.

(7) Turn the NAV SIM dial in either direction

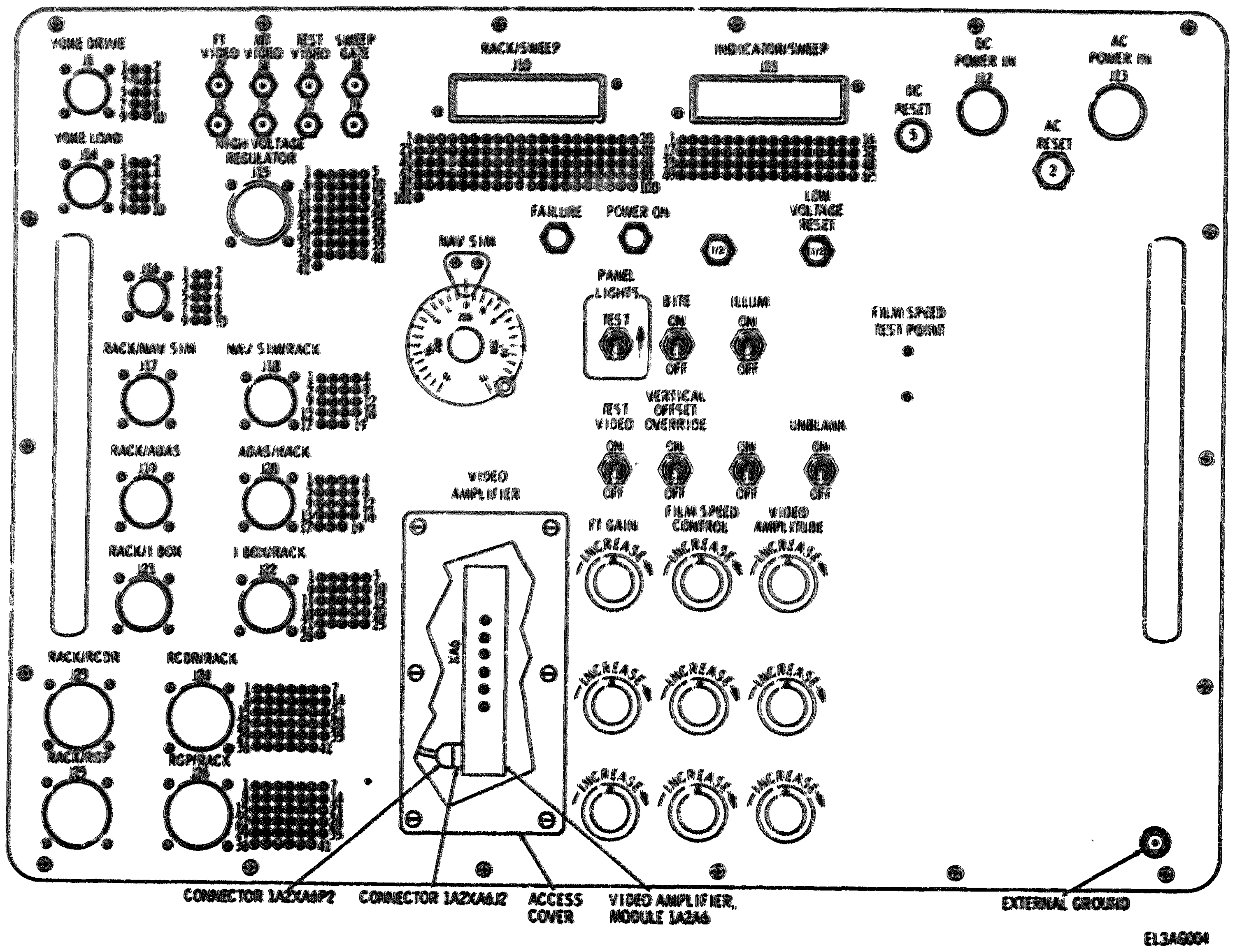


Figure 3-5. Test Set Subassembly MX-8633A/APS-94D, Unit 1A2, front panel parts location.

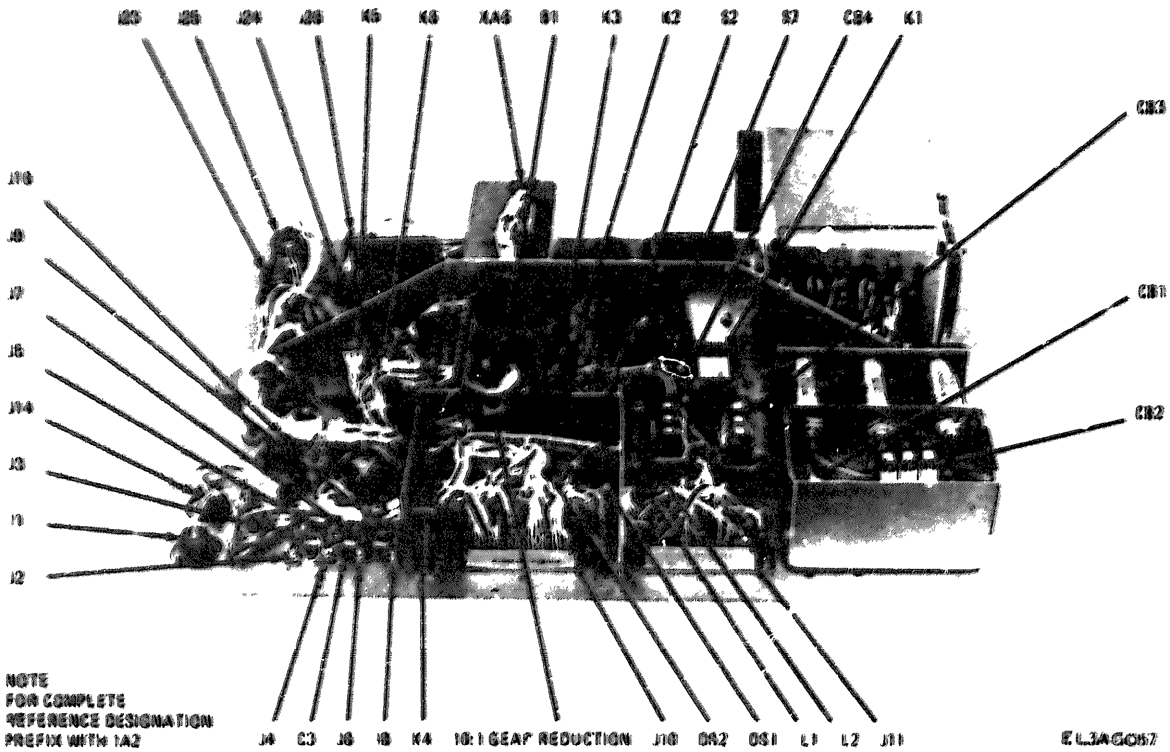


Figure 3-6. Test Set Subassembly Mx-8638A/APS-94D, Unit 1A2, rear chassis top view, parts location.

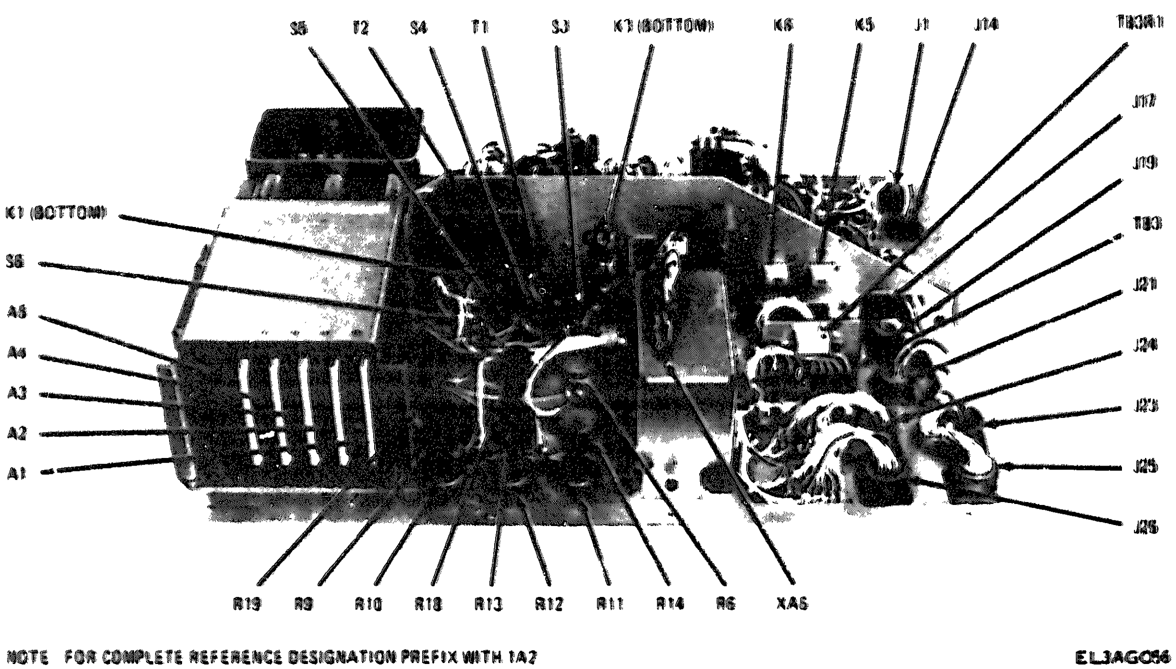


Figure 3-7. Test Set Subassembly MX-8638A/APS-94D, Unit 1A2 rear chassis bottom view, parts location

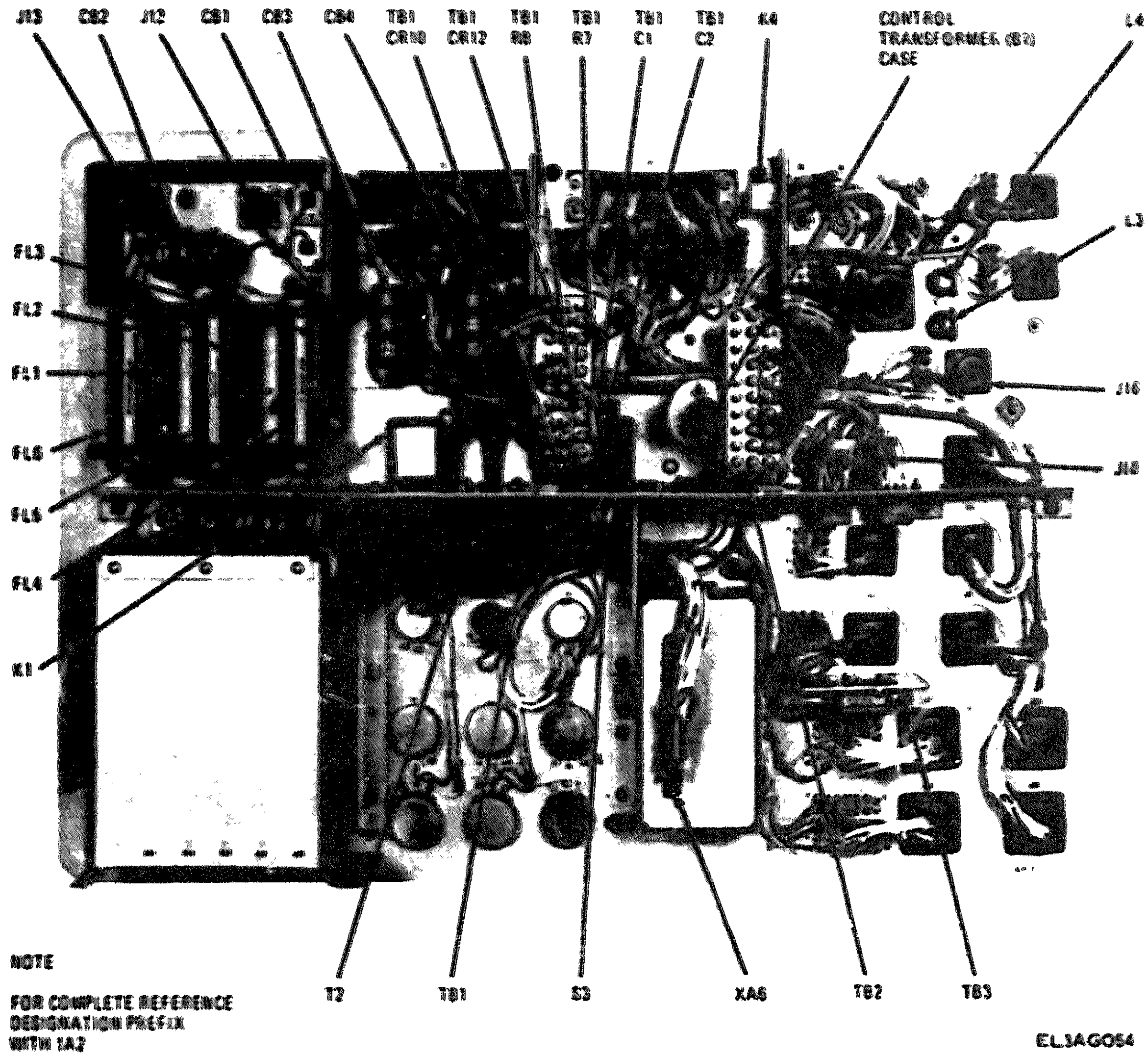


Figure 3-8. Test Set Subassembly MX8638A/APS-94D, Unit 1A2, rear chassis parts location

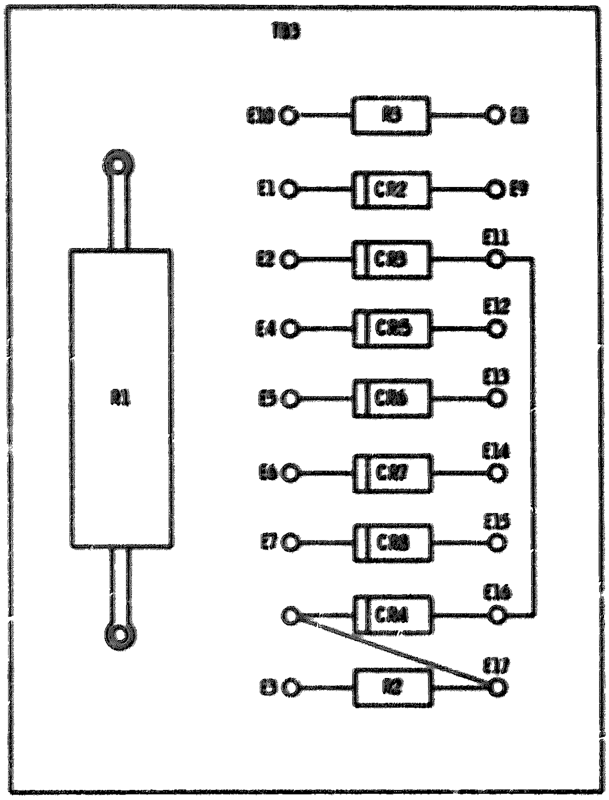


Figure 3-9. Terminal board 1A2TB3, parts location.

(ten revolutions maximum) to obtain maximum deflection of the multimeter.

(8) Reassemble the locking mechanism of the NAV SIM dial.

(9) Turn the NAV SIM dial to 0 and lock the dial at this setting with the dial lock.

(10) Loosen the three clamp screws that secure the case of synchro motor 1A2B1 (fig. 3-8).

(11) Observe the multimeter and slowly turn the case of motor 1A2B1 to produce a maximum deflection on the mulitmeter.

(12) Tighten the three clamp screws that secure the case of motor 1A2B1.

(13) Reconnect cable W4 to NAV SIM/RACK connector 1A2J18.

3-42. Servocontrol Synchro Fine Calibration

a. Test Equipment Required. The multimeter is the only test equipment required for the calibration procedure.

b. Primary Procedures. Perform instructions given in paragraph 3-41*b*.

c. Test Setup and Conditions. Same as described in paragraph 3-41*c*.

d. Initial Test Equipment Calibration. Same as described in paragragh 3-41*d*.

e. Calibration Procedure.

(1) Disconnect cable W4 from NAV SIM/RACK connector 1A2J18.

(2) Perform the equipment connections as illustrated in B, figure 3-1.

(3) Perform instructions (3) through (5) in paragraph 3-41*e*.

(4) Turn the NAV SIM dial on unit 1A2 to 0 and lock the dial at this setting with the dial lock.

(5) Loosen the three clamp screws (fig. 3-8) that secure the case of synchro motor 1A2B1.

(6) Observe the multimeter and slowly turn the

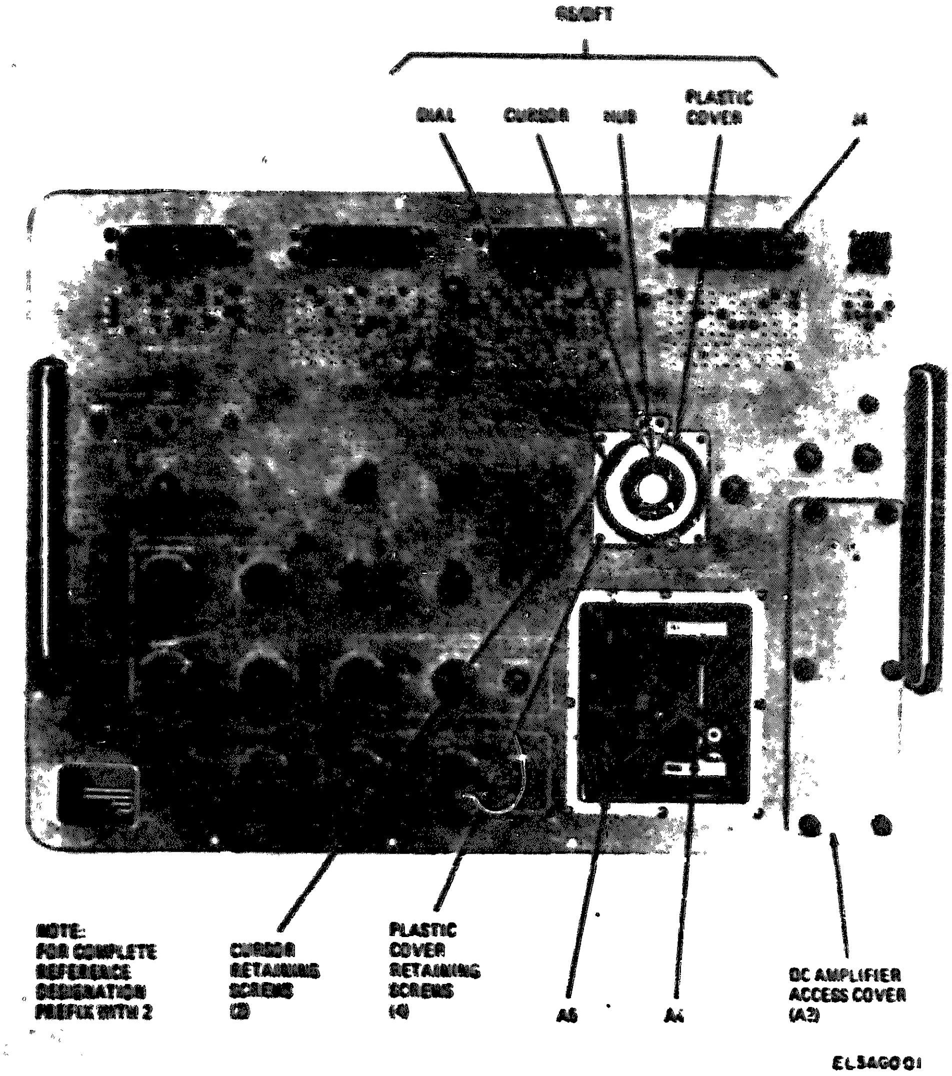


Figure 3-10. Test Set Subassembly MX-8632A/APS-94D, Unit 2, front panel, parts location.

case of synchro motor 1A2B1 to produce minimum deflection on the mulitmeter.

(7) Tighten the three clamp screws that secure the case of the synchro motor 1A2B1.

(8) Unlock the NAV SIM dial and carefully rock the dial to identify the precise position of the multimeter null.

(9) Lock the dial at the position determined in (8) above.

(10) Loosen the screws that secure the indication reference for the dial and move the indication reference so that the dial indicates 0; then tighten the screws.

(11) Reconnect cable W4 to NAV SIM/RACK connector 1A2J18.

3-43. GS/DFT Dial Calibration

a. Test Equipment Required. None required.

b. Preliminary Procedures. Perform instructions given in (3) through (6) of paragraph 3-41*b*.

c. Test Setup and Conditions. Same as described in paragraph 3-41*c*.

d. Calibration Procedures.

CAUTION

Do not attempt to turn the GS/DFT dial manually while the dial is secured to the dial shaft. Equipment damage may result.

(1) Perform instructions (3) and (4) of paragraph 3-41*e*.

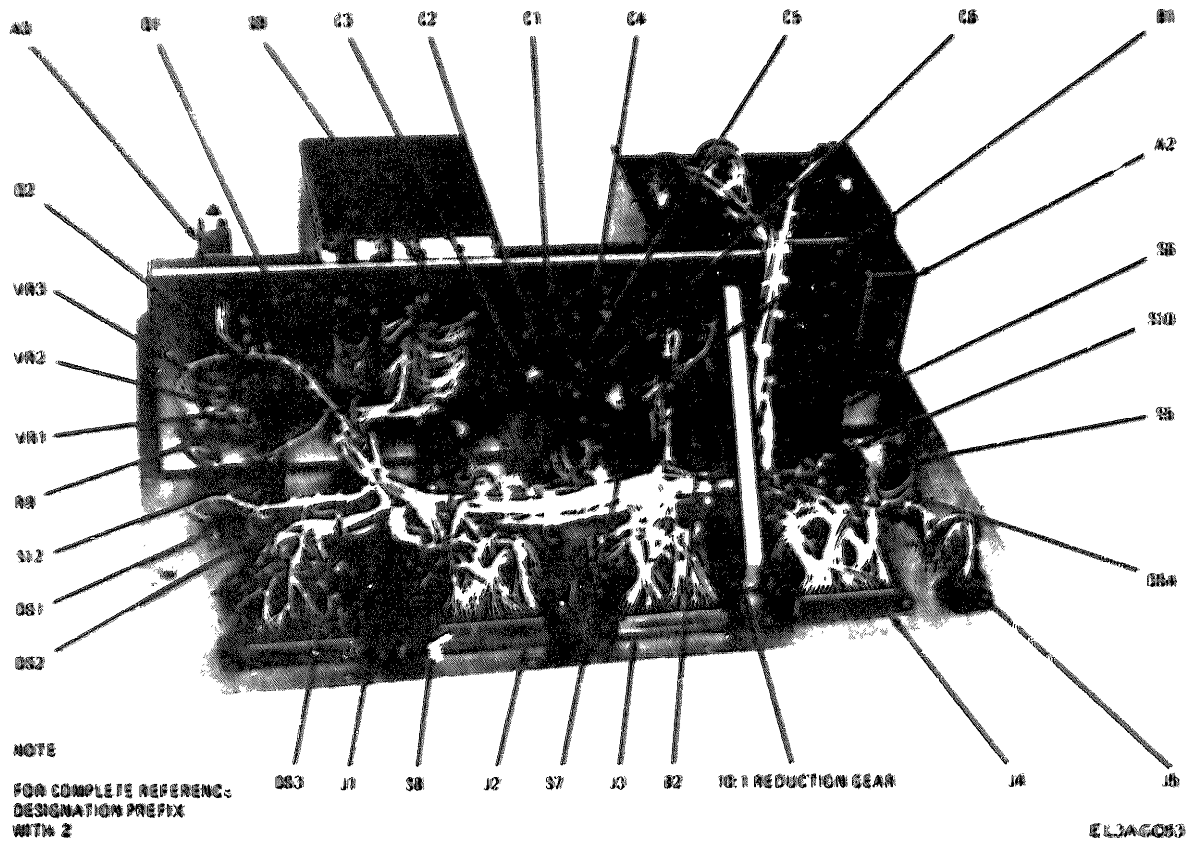


Figure 3-11. Test Set Subassembly MX-8639A/APD-94D, Unit 2 rear chassis new, parts location

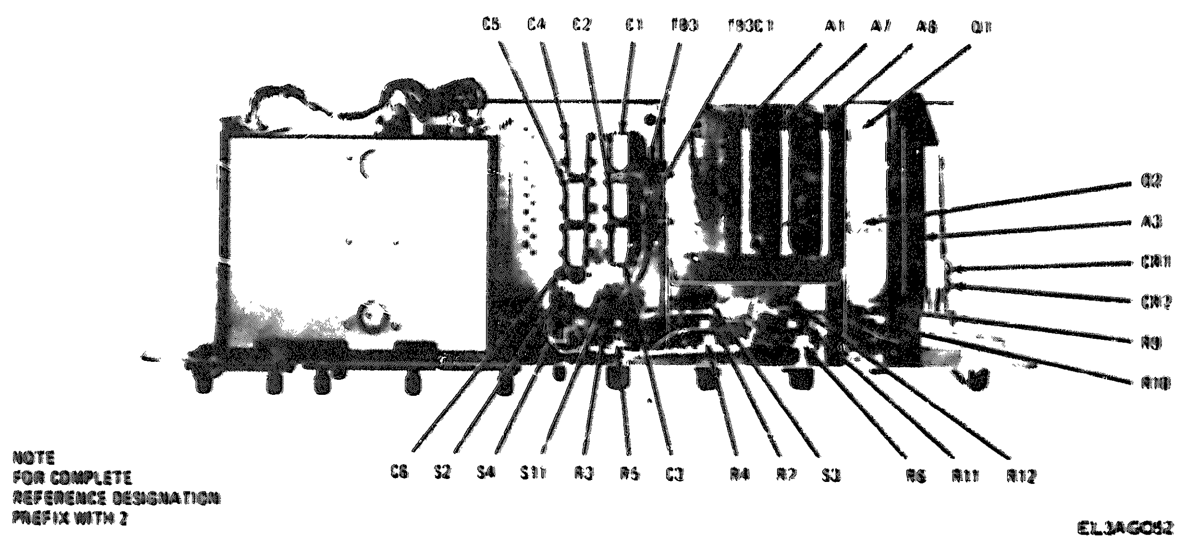


Figure 3-12. Test Set Subassembly MX-8639A/APS-94D, Unit 2, bottom chassis new, parts location

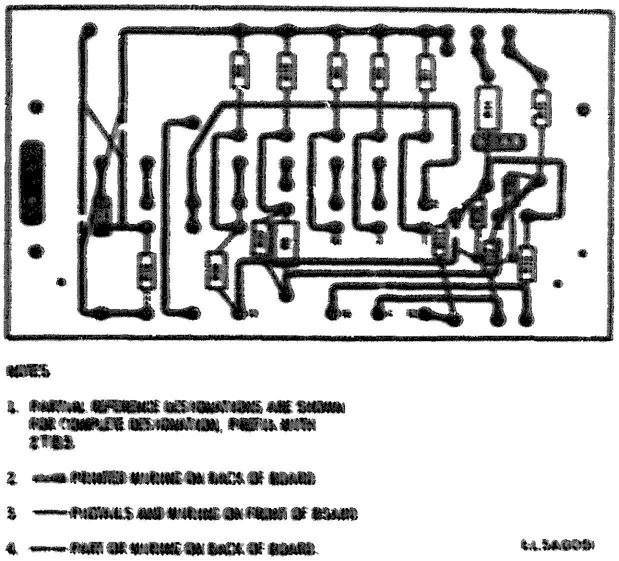


Figure 3-13. Terminal board parts locations

(2) Wait 5 minutes for the equipment to warm up and stabilize.

(3) Make the following control adjustments on unit 2:

(a) Turn the SERVO LOOP switch to DFT.

(b) Set the GS/DFT DRIVE switch to ON.

(c) Set the NAVIGATION switch to AUTO.

(4) Remove the indication reference for the GS/DFT dial and the dial plastic cover.

(5) Install the indication reference for the dial.

(6) Loosen the setscrews in the dial hub and slide the dial off the dial shaft.

(7) Align 0 on the dial and the indexing line on the indication reference for the dial; then slide the dial back onto the dial shaft and tighten the setscrews in the dail hub.

(8) Remove the indication reference for the dial.

(9) Install the dial plastic cover and indication reference for the dial, taking care to align the indication reference index line with the dial 0.

Section IV. DIRECT SUPPORT TESTING PROCEDURES

3-44. General

a. Testing procedures are prepared for use by organizations responsible for direct support maintenance of electronic equipment to determine the acceptability of repaired electronic equipment. These procedures set forth specific requirements that repaired electronic equipment must meet before it is returned to the using organization. The testing procedures include performing a physical test and inspection on the equipment and an electrical test.

b. The tests in this section are arranged to be performed in the sequence given. Comply with instructions preceding each test. Perform each step of each test procedure in sequence. For each step, perform all the actions required in the *Control settings* columns; then perform each specific test procedure and verify it against its performance standard.

3-45. Physical Tests and Inspections

a. General. The following physical tests cover each component of test set group and are divided into three groups covering the test set group as follows: Test Set Subassembly MX-8636A/APS-94D (indicator simulator unit 1A1) (lower); (indicator simulator unit 1A2) (upper); and Test Set Subassembly MX-8639A/APS-94D (generator simulator unit 2). The physical tests and inspection are to be performed on each component being tested before it is connected into its test setup. The procedure is intended to minimize the possibility of damage caused by the application of bench power.

b. Test Equipment Required. None required.

c. Test Connections and Conditions. Prepare the equipment for test as directed below.

(1) Equalize the inside-to-outside air pressure by

depressing the red button at the center of breather valve on each test set group case.

(2) Pull up on each of the eight cover latches and free latches from cover.

(3) Separate the case covers and arrange the equipment on a suitable bench that is capable of accommodating the test set group.

3-46. Indicator Simulator, **Unit 1A1, Physical** Test and Inspections

Perform the indicator simulator, unit 1A1, physical test and inspection as described in table 3-38 below.

Table 3-38. Indicator Simulator. Unit 1A1, Indicator Physical Test and Inspection

Step No.	Control Settings: Test Equipment	Control Settings: Equipment Under Test	Test Procedure	Performance Standard
1	None	Controls may be in any position.	*a.* Inspect all control and mechanical assemblies for loose or missing screws, bolts, and nuts. *b.* Inspect jacks J1 through J11 for damage	*a.* Screws, bolts, and nuts must be tight, none missing. *b* No looseness or damage evident.
2	None	Controls may be in any position	*a.* Remove 4 screws, lockwashers, and washers securing the filter housing to control panel. Inspect remoed parts *b* Remove the filter element and visually inspect it. After inspection, replace all parts removed	*a* No mechanical damage evident, rfi gasket not cracked, torn, or pinched *b* dirt or foreign objects visible
3	None	Controls may be in any position	Remove low voltage regulator cover plate and inspect low voltage regulator subassembly 1A1A4 for secure positioning in mating connector Replace all parts removed.	Subassembly 1A1A4 is secure in connector
4	None	Controls may be in any position	Remove lens cover from HIGH VOLTAGE ON indicator lamp Inspect the lamp for secureness in their connectors. Replace lens cover after inspection	Lamp secure in connector, lens cover intact.

3-47. Indicator Simulator, Unit 1A2, Physical Test and Inspection

Perform the indicator simulator, unit 1A2, physical test and inspection as described in table 3-39 below.

Table 3-39. Indicator Simulator Unit 1A2, Physical Test and Inspection

Control Settings: Test Equipment	Control Settings: Equipment Under Test	Test Procedure	Performance Standard
None	Controls may be in any position	*a* Inspect all controls, mechanical assemblies and panels for loose or missing screws, bolts, and nuts *b* Inspect jacks J1 through J26 for evidence of damage	a Screws, bolts, and nuts must be tight: none missing *b* No looseness or damage evident
None	Controls may be in any position	Remove screws from VIDEO AMPLIFIER access cover, remove cover and inspect assembly 1A2A6 for security in its mating connector Replace all parts removed	Assembly 1A2A6 is secure in its connector All removed parts now secured.

Table 3-39. Indicator Simulator, Unit 1A2, Physical Test and Inspection-Continued

Step No.	Control Settings		Test Procedure	Performance Standard
	Test Equipment	Equipment Under Test		
3	None	Controls may be in any position	*a.* Turn the NAV SIM control from one extreme to the other and back. *b.* Actuate (in the direction of the arrow) and release the PANEL LIGHTS TEST switch. *c* Operate the following ON/OFF switches· BITE, ILLUM, TEST VIDEO, VERTICAL OFFSET OVERRIDE, HIGH VOLTAGE and UNBLANK. *d* Operate the following controls throughout their full range of mechanical travel FT GAIN, FILM SPEED CONTROL, and VIDEO AMPLITUDE	*a.* Control operates freely in both directions throughout its range. *b* Switch operates freely and returns to its normal operating position *c* All switches operate freely *d* All controls operate freely throughout the full range of mechanical travel, no roughness or binding evident

3-48. Generator Simulator, Unit 2, Physical Test and Inspection

Perform the generator simulator, unit 2, physical test and inspection as described in table 3-40 below.

Table 3-40. Generator Simulator, Unit 2, Physical Test and Inspection

Step No.	Control Settings		Test Procedure	Performance Standard
	Test Equipment	Equipment Under Test		
1	None	Controls may be in any position.	*a.* Inspect all controls and mechanical assemblies for loose or missing screws, bolts, and nuts. *b* Inspect jacks J1 through J5 for damage	*a* Screws, bolts, and nuts must be tight, none missing *b* Jacks show no evidence of looseness or damage
2	None	Controls may be in any position	Remove screws securing the SERVO AMPLIFIER and SWEEP GENERATOR access covers and inspect the subassemblies for secureness in their mating connectors Replace covers after inspection.	Subassemblies secure in their mating connectors, covers intact
3	None	Controls may be in any position.	Remove screws from HORIZONTAL AMPLIFIER access cover and remove cover. Inspect subassembly 2A2 for secureness in its mating connector Replace cover after inspection.	Subassembly 2A2 is secure in its mating connector
4	None	Controls may be in any position.	*a.* Actuate (in the direction of the arrow) and release the PANEL LIGHTS TEST switch. *b* Operate the POWER ON/OFF switch to both positions. *c* Operate the NAVIGATION switch to all three positions.	*a.* Switch operates freely and returns to its normal operating position. *b* Switch operates freely in both directions *c* Switch operates freely in all three positions.

Table 3-40. Generator Simulator, Unit 2, *Physical Test* and Inspection-Continued

Step No.	Control Settings		Test Procedure	Performance Standard
	Test Equipment	Equipment Under Test		
			d. Operate the following controls to all their panel-indicated positions· RANGE, ANTENNA, SERVO LOOP, DISPLAY, DRIFT ANGLE, GS/DFT DRIVE, and HORIZONTAL AMPLIFIER and VERTICAL AMPLIFIER controls.	d All controls operate freely to each of their panel-indicated positions
			e Operate the following controls throughout their full range of mechanical travel. OFFSET and INTENSITY controls	e All controls operate freely throughout their range of mechanical travel, no roughness or binding evident

3-49. Electrical Tests

a. Tools and Test Equipment Required.

(1) Multimeter AN/USM-223.

(2) Oscilloscope AN/USM-281C.

(3) Transformer, Variable Power, General Radio Type M2G3.

(4) Voltmeter, Digital AN/GSM-64B.

(5) Generator, Signal SG-1105/G.

(6) Tool Kit, Electronic Equipment TK-105/G.

(‘7) Termination, 100-ohm HP 10100B.

b. Test Conditions and Connections.

(1) Arrange the equipment on a workbench in the following left-to-right order. Indicator simulator (unit lA2), generator simulator (unit 2), and indicator simulator (unit 1A1).

(2) Connect interconnecting cables to the test set group as illustrated in figure FO-4.

(3) Perform the preliminary procedures given in paragraph 3-15.

c. ***Procedure.*** The electrical tests for the test set group are identical to the bench tests given in Section II, Troubleshooting. Perform all the bench tests in Section II in the sequence given.

Section V. WIRE LIST FOR TEST SET GROUP, INDICATOR, RADAR OQ-63A/APS-94D

3-50. General

This section contains the wire lists for the test set group. The wire lists cover the wiring for the three units of the test set group. Each list presents point-to-point (from and to) data in alphanumerical sequence and the wire number. The lists are *also* double-ended, that is, any one wire appears twice in the left hand column with the ***From*** and To locations (wire ends) occurring in alphanumerical sequence. Wired in subassemblies are covered by individual illustrations which are referenced in the appropriate troubleshooting paragraphs.

3-51. Test Set Subassembly MX-8638A/APS-94D, Unit 1A1 Wire List

The wire list for unit 1A1 is presented in table 3-41. The ***wire*** list will be an aid to the repairman when testing or troubleshooting unit 1A1.

Table 3-41. Test Set Subassembly MX-8638A/APS-94D, Unit 1A1, Wire List

From	To	Wire No	From	To	Wire No.
A5–E1	E–2	182	A6–E5	E–17	180
A5–E4	XA2–C	181	B1–A	E–6	215
A5–E5	E–17	183	B1–B	E–7	216
A6–E1	E–1	178	B1–C	E–8	217
A6–E4	XA2–3	179			

Table 3-41 Test Set Subassembly MX-8638A/APS-94D, Unit 1A1, Wire Last- Continued

From	To	Wire No.	From	To	Wire No.
E-1	A6-E1	178	J1-TP1	E-6	13
E-2	A5-E1	182	J1-TP1	T1-1	228
E-3	XA2-D	200	J1-TP1	J1-A	1
E-4	XA2-B	199	J1-TP2	E7	14
E-5	XA2-P	194	J1-TP2	J1-B	2
E-6	P1-A	215	J1-TP2	T1-2	221
E-6	XA1-A	16	J1-TP3	E-8	15
E-6	J1-TP1	13	J1-TP3	J1-C	3
E-7	XA1-B	17	J1-TP4	NC	
E-7	B1-B	216	J1-TP5	NC	
E-7	J1-TP2	14	J1-TP6	XA2-E	15A
E-8	XA1-C	18	J1-TP6	J1-H	5
E-8	B1-C	217	J1-TP7	NC	
E-8	J1-TP3	15	J1-TP8	XA2-5	15B
E-9	J3-TP10	83	J1-TP9	NC	
E-9	J3-TP8	81	J1-TP10	XA1-K	21
E-9	J3-TP12	85	J1-TP10	J1-K	6
E-10	J4-TP19	118	J1-TP11	J1-L	7
E-10	J4-TP41	123	J1-TP11	XA1-L	22
E-10	XDS2-2	220	J1-TP12	XA2-6	15C
E-11	J5-TP13	148	J1-TP12	J1-M	8
E-11	J5-TP14	149	J1-TP13	J1-N	9
E-11	J5-TP25	154	J1-TP13	XA1-N	24
E-11	XDS1-2	218	J1-TP14	J1-P	10
E-12	J7-TP3	159	J1-TP14	XA1-P	25
E-12	J7-TP15	161	J1-TP15	J1-R	26
E-12	S1-3	222	J1-TP16	NC	
E-13	J9-TP11	176	J1-TP17	NC	
E-13	J9-TP12	177	J1-TP18	J1-U	12
E-14	R1-2	221	J1-TP18	XA1-U	27
E-15	XA6-A	186	J1-TP19	NC	
E-16	XA2-A	197	J1-TP20	NC	
E-16	XA2-22	198	J1-TP21	NC	
E-16	PS1-2	227	J1-TP22	NC	
E-17	A5-E5	183	J1-TP23	NC	
E-17	A6-E5	180	J1-TP24	NC	
E-18	J2-TP3	49	J1-TP25	NC	
E-18	J2-TP19	53	J1-TP26	NC	
J1-A	J1-TP1	1	J2-A	J2-TP1	28
J1-B	J1-TP2	2	J2-B	J2-TP2	29
J1-C	J1-TP3	3	J2-C	J2-TP3	30
J1-D	NC		J2-D	NC	
J1-E	NC		J2-E	NC	
J1-F	J1-TP6	4	J2-F	J2-TP6	31
J1-G	NC		J2-G	NC	
J1-H	J1-TP8	5	J2-H	NC	
J1-J	NC		J2-J	NC	
J1-K	J1-TP10	6	J2-K	NC	
J1-L	J1-TP11	7	J2-L	J2-TP11	32
J1-M	J1-TP12	8	J2-M	J2-TP12	33
J1-N	J1-TP13	9	J2-N	J2-TP13	34
J1-P	J1-TP14	10	J2-P	J2-TP14	35
J1-R	J1-TP15	11	J2-R	J2-TP15	36
J1-S	NC		J2-S	J2-TP16	37
J1-T	NC		J2-T	J2-TP17	38
J1-U	J1-TP18	12	J2-U	J2-TP18	39
J1-V	NC		J2-V	J2-TP19	40
J1-W	NC		J2-W	J2-TP20	41
J1-X	NC		J2-X	J2-TP21	42
J1-Y	NC		J2-Y	J2-TP22	43
J1-Z	NC		J2-Z	J2-TP23	44
J1-a	NC		J2-a	J2-TP24	45
J1-b	NC		J2-b	NC	
J1-c	NC		J2-c	J2-TP26	46

Table 3-41. Test Set Subassembly MX-8638A/APS-94D, Unit 1A1, Wire List-Continued

From	To	Wire No.	From	To	Wire No.
J2-d	NC		J3-TP1	XA2-S	74
J2-e	NC		J3-TP1	J3-A	55
J2-f	NC		J3-TP2	XA2-Z	75
J2-g	NC		J3-TP2	J3-A	55
J2-h	NC		J3-TP3	J3-TP6	76
J2-i	NC		J3-TP3	J3-C	57
J2-j	NC		J3-TP4	T1-5	77
J2-k	NC		J3-TP4	J3-D	58
J2-l	NC		J3-TP5	XA2-9	78
J2-m	NC		J3-TP5	J3-E	59
J2-n	NC		J3-TP6	XA2-F	79
J2-p	NC		J3-TP6	J3-F	60
J2-r	NC		J3-TP6	J3-TP3	76
J2-s	NC		J3-TP7	J3-G	61
J2-t	NC		J3-TP7	XA2-1	80
J2-TP1	J2-A	28	J3-TP8	J3-H	62
J2-TP1	XA6-U	47	J3-TP8	E9	81
J2-TP2	XA6-W	48	J3-TP9	XA2-S	82
J2-TP2	J2-B	29	J3-TP9	J3-J	63
J2-TP2	J2-TP12	54	J3-TP10	J3-K	64
J2-TP3	J2-C	30	J3-TP10	E9	83
J2-TP3	E-18	49	J3-TP11	XA2-R	84
J2-TP6	R1-1	50	J3-TP11	J3-L	65
J2-TP6	J2-F	31	J3-TP12	E9	85
J2-TP11	E-18	51	J3-TP12	J3-M	66
J2-TP11	J2-L	32	J3-TP13	J3-N	67
J2-TP12	J5-TP19	52	J3-TP14	J3-P	68
J2-TP12	J2-M	33	J3-TP15	J3-R	69
J2-TP12	J2-TP2	54	J3-TP16	NC	
J2-TP13	J2-N	34	J3-TP17	NC	
J2-TP14	J2-P	35	J3-TP18	NC	
J2-TP15	J2-R	36	J3-TP19	NC	
J2-TP16	J2-S	37	J4-A	J4-TP1	86
J2-TP17	J2-T	38	J4-B	J4-TP2	87
J2-TP18	J2-U	39	J4-C	J4-TP3	88
J2-TP18	J5-TP8	143	J4-D	J4-TP4	89
J2-TP19	E-18	53	J4-F	J4-TP6	90
J2-TP19	J2-V	40	J4-G	J4-TP7	91
J2-TP19	J5-TP9	144	J4-H	NC	
J2-TP20	J2-W	41	J4-J	J4-TP9	92
J2-TP21	J2-X	42	J4-K	J4-TP10	93
J2-TP22	J2-Y	43	J4-L	J4-TP11	94
J2-TP23	J2-Z	44	J4-M	J4-TP12	95
J2-TP24	J2-a	45	J4-N	J4-TP13	96
J2-TP26	J2-c	46	J4-P	J4-TP14	97
J3-A	J3-TP1	55	J4-R	J4-TP15	98
J3-B	J3-TP2	56	J4-S	J4-TP16	99
J3-C	J3-TP3	57	J4-T	J4-TP17	100
J3-D	J3-TP4	58	J4-U	J4-TP18	101
J3-E	J3-TP5	59	J4-V	J4-TP19	102
J3-F	J3-TP6	60	J4-W	J4-TP20	103
J3-G	J3-TP7	61	J4-X	NC	
J3-H	J3-TP8	62	J4-Y	NC	
J3-J	J3-TP9	63	J4-Z	NC	
J3-K	J3-TP10	64	J4-a	J4-TP24	104
J3-L	J3-TP11	65	J4-b	J4-TP25	105
J3-M	J3-TP12	66	J4-c	NC	
J3-N	J3-TP13	67	J4-d	NC	
J3-P	J3-TP14	68	J4-e	J4-TP28	106
J3-R	J3-TP15	69	J4-f	J4-TP29	107
J3-S	NC		J4-g	J4-TP30	108
J3-T	NC		J4-h	J4-TP31	109
J3-U	NC		J4-j	NC	
J3-V	NC		J4-k	NC	

Table 3-41. Test Set Subassembly MX-8638A/APS-94D, Unit **1A1,** Wire List - Continued

From	To	Wire No.
J4-l	NC	
J4-m	NC	
J4-n	NC	
J4-p	NC	
J4-r	J4-TP39	110
J4-s	NC	
J4-t	J4-TP41	111
J4-TP1	J4-A	86
J4-TP2	J4-B	87
J4-TP3	J4-C	88
J4-TP4	J4-D	89
J4-TP5	NC	
J4-TP6	XA2-16	112
J4-TP6	J4-F	90
J4-TP6	J4-TP16	116
J4-TP7	XA2-Z	113
J4-TP7	J4-G	91
J4-TP8	NC	
J4-TP9	J4-J	92
J4-TP10	J4-K	93
J4-TP11	J4-L	94
J4-TP12	J4-M	95
J4-TP13	XDS2-1	114
J4-TP13	J4-N	96
J4-TP14	XA6-B	115
J4-TP14	J4-P	97
J4-TP15	J4-R	98
J4-TP16	J4-TP6	116
J4-TP16	J4-5	99
J4-TP17	T1-5	117
J4-TP17	J4-T	100
J4-TP18	J4-U	101
J4-TP19	E10	118
J4-TP19	J4-V	102
J4-TP20	J4-W	103
J4-TP21	NC	
J4-TP22	NC	
J4-TP23	NC	
J4-TP24	J4-a	104
J4-TP25	J4-b	105
J4-TP26	NC	
J4-TP27	NC	
J4-TP28	J4-e	106
J4-TP29	J4-f	107
J4-TP30	J4-g	108
J4-TP31	J4-h	109
J4-TP32	NC	
J4-TP33	NC	
J4-TP34	NC	
J4-TP35	NC	
J4-TP36	NC	
J4-TP37	NC	
J4-TP38	NC	
J4-TP39	J4-r	110
J4-TP40	NC	
J4-TP41	J4-t	111
J5A	J5-TP1	124
J5B	J5-TP2	125
J5C	J5-TP3	126
J5D	NC	
J5E	NC	
J5F	NC	
J5G	NC	
J5H	J5-TP8	127
J5J	J5-TP9	128
J5K	J5-TP10	129
J5L	J5-TP11	130
J5M	J5-TP12	131
J5N	J5-TP13	132
J5P	J5-TP14	133
J5R	NC	
J5S	NC	
J5T	NC	
J5U	J5-TP18	134
J5V	J5-TP19	135
J5W	NC	
J5X	NC	
J5Y	J5-TP22	136
J5Z	J5-TP23	137
J5a	J5-TP24	138
J5b	J5-TP25	139
J5c	NC	
J5-TP1	J5-A	[illegible]
J5-TP1	PSI-3	140
J5-TP2	J5-B	125
J5-TP2	J5-TP3	142
J5-TP2	PSI-4	141
J5-TP3	J5-TP2	142
J5-TP3	J5-C	126
J5-TP8	J5-H	127
J5-TP9	J5-J	128
J5-TP10	J5-K	129
J5-TP11	J5-L	130
J5-TP12	J5-M	131
J5-TP13	J5-N	132
J5-TP14	J5-P	133
J5-TP16	NC	
J5-TP17	NC	
J5-TP18	J5-U	134
J5-TP19	J5-V	135
J5-TP19	J2-TP12	53
J5-TP20	NC	
J5-TP21	NC	
J5-TP22	J5-Y	136
J5-TP23	J5-Z	137
J5-TP24	J5-a	138
J5-TP25	J5-b	139
J5-TP26	NC	
J7-A	J7-TP1	155
J7-B	NC	
J7-C	J7-TP3	157
J7-D	NC	
J7-E	NC	
J7-F	NC	
J7-G	NC	
J7-H	NC	
J7-J	NC	
J7-K	NC	
J7-L	NC	
J7-M	J7-TP12	156
J7-N	NC	
J7-P	NC	
J7-R	SHIELD	
J7-5	NC	
J7-TP1	J7-A	155
J7-TP1	XA6-P	158
J7-TP3	E12	159
J7-TP3	J7-C	157

Table 3-41. Test Set Subassembly MX8638A/APD-94D Unit 1A1, Wire List - Continued

From	To	Wire No.	From	To	Wire No.
J7-TP12	XA6-V	160	NC	J2-G	
J7-TP12	J7-M	156	NC	J2-H	
J7-TP15	E-12	161	NC	J2-J	
J7-TP15	SHIELD OF M	160A	NC	J2-K	
J7-TP17	SHIELD OF M	155B	NC	J2-b	
J9-A	J9-TP1	162	NC	J2-d	
J9-B	J9-TP2	163	NC	J2-e	
J9-C	NC		NC	J2-f	
J9-D	J9-TP4	164	NC	J2-g	
J9-E	NC		NC	J2-h	
J9-F	J9-TP6	165	NC	J2-i	
J9-G	NC		NC	J2-j	
J9-H	NC		NC	J2-k	
J9-J	NC		NC	J2-l	
J9-K	NC		NC	J2-m	
J9-L	J9-TP11	166	NC	J2-n	
J9-L	J9-TP12	167	NC	J2-P	
J9-N	J9-TP13	168	NC	J2-r	
J9-P	J9-TP14	169	NC	J2-s	
J9-R	J9-TP15	170	NC	J2-t	
J9-S	J9-TP16	171	NC	J3-S	
J9-T	J9-TP17	172	NC	J3-T	
J9-U	J9-TP18	173	NC	J3-U	
J9-V	J9-TP19	174	NC	J3-V	
J9-TP1	J9-A	162	NC	J4-H	
J9-TP1	XA6-B	175	NC	J4-X	
J9-TP2	J9-B	175	NC	J4-Y	
J9-TP3	NC		NC	J4-Z	
J9-TP4	J9-D	164	NC	J4-c	
J9-TP5	NC		NC	J4-d	
J9-TP6	J9-F	165	NC	J4-j	
J9-TP7	NC		NC	J4-k	
J9-TP8	NC		NC	J4-l	
J9-TP9	NC		NC	J4-m	
J9-TP10	NC		NC	J4-n	
J9-TP11	E-13	176	NC	J4-p	
J9-TP11	J9-L	166	NC	J4-s	
J9-TP12	J9-M	167	NC	J5-c	
J9-TP12	E-13	177	NC	J5-d	
J9-TP13	J9-N	168	NC	J5-E	
J9-TP14	J9-P	169	NC	J5-F	
J9-TP15	J9-R	170	NC	J5-G	
J9-TP16	J9-S	171	NC	J5-R	
J9-TP17	J9-T	172	NC	J5-S	
J9-TP18	J9-U	173	NC	J5-T	
J9-TP19	J9-V	174	NC	J5-W	
L1-1	XA2-Y	205	NC	J5-X	
L1-2	XA2-20	210	NC	J5-TP4	
NC	J1-W		NC	J5-TP5	
NC	J1-X		NC	J5-TP6	
NC	J1-Y		NC	J5-TP7	
NC	J1-Z		NC	J5-TP15	
NC	J1-a		NC	J5-TP16	
NC	J1-b		NC	J5-TP17	
NC	J1-c		NC	J5-TP19	
NC	J2-d		NC	J5-TP20	
NC	J1-D		NC	J5-TP21	
NC	J1-E		NC	J5-TP26	
NC	J1-G		NC	J7-B	
NC	J1-J		NC	J7-D	
NC	J1-S		NC	J7-E	
NC	J1-T		NC	J7-F	
NC	J1-V		NC	J7-G	
NC	J2-E		NC	J7-H	

Table 3-41. Test Set Subassembly MX-8638A/APS-94D, Unit 1A1, Wire List-Continued

From	To	Wire No.	From	To	Wire No.
NC	J7-J		XA1-Z	NC	
NC	J7-K		XA1-a	NC	
NC	J7-L		XA1-b	NC	
NC	J7-N		XA2-A	NC	
NC	J7-P		XA2-A	E-16	197
NC	J7-S		XA2-A	XA2-1	195
NC	J9-C		XA2-A	E-16	197
NC	J9-E		XA2-B	E-4	199
NC	J9-G		XA2-C	A5-E4	181
NC	J9-H		XA2-D	E3	200
NC	J9-J		XA2-E	XA6-U	193
NC	J9-K		XA2-F	J3-TP6	79
PS1-1	S2-1	223	XA2-F	XA2-L	201
PS1-1	XDS1-2	219	XA2-G	NC	
PS1-2	E16	227	XA2-H	S3-3	202
PS1-3	J5-TP1	140	XA2-J	T1-6	203
PS1-4	J5-TP2	141	XA2-K	NC	
R2-1	J5-TP10	145	XA2-L	J4-TP29	120
R2-2	J5-TP11	146	XA2-L	XA2-M	206
R2-3	J5-TP12	147	XA2-M	T1-7	211
R3-1	J5-TP22	151	XA2-M	S3-1	212
R3-2	J5-TP23	152	XA2-M	XA2-L	206
R3-3	J5-TP24	153	XA2-N	NC	
SHIELD OF A	SHIELD OF M	155B	XA2-P	E-5	194
SHIELD OF e & f	J4-TP28	119	XA2-R	J3-TP11	84
SHIELD OF M	J7-R	156A	XA2-S	XA2-15	213
SHIELD OF M	SHIELD OF A	158B	XA2-S	J3-TP9	82
S1-W	XA6-D	189	XA2-S	J3-TP1	74
S1-1	XA6-E	188	XA2-T	XA6-Y	191
S1-2	XA6-E	190	XA2-U	NC	
S3-1	XA2-M	212	XA2-V	T1-9	204
S3-2	XA2-6	207	XA2-W	NC	
S3-3	XA2-H	202	XA2-X	NC	
S3-4	XA2-7	208	XA2-Y	L1-1	205
T1-5	J3-TP4	77	XA2-Z	J3-TP2	75
T1-5	J4-TP17	117	XA2-Z	J4-TP7	113
T1-6	XA2-J	203	XA2-Z	XA2-22	196
T1-7	S3-1	225	XA2-1	J3-TP7	80
T1-7	XA2-M	211	XA2-1	XA2-A	195
T1-8	XA2-18	209	XA2-2	NC	
T1-9	XA2-V	204	XA2-3	A6-E4	179
XA1-A	E6	16	XA2-4	NC	
XA1-B	E7	17	XA2-5	J1-TP8	15B
XA1-C	E8	18	XA2-5	J5-TP18	150
XA1-D	NC		XA2-5	XA6-W	192
XA1-E	NC		XA2-6	J1-TP12	15C
XA1-F	XA6-U	19	XA2-6	S1-2	207
XA1-G	NC		XA2-7	S1-4	208
XA1-H	XA6-W	20	XA2-8	NC	
XA1-J	NC		XA2-9	J3-TP5	78
XA1-K	J1-TP10	21	XA2-9	J4-TP30	121
XA1-L	J1-TP11	22	XA2-10	S3-W	226
XA1-M	XA6-X	23	XA2-11	NC	
XA1-N	J1-TP13	24	XA2-12	J4-TP39	122
XA1-P	J1-TP14	25	XA2-13	NC	
XA1-R	J1-TP15	26	XA2-14	NC	
XA1-S	NC		XA2-15	XA2-16	214
XA1-T	NC		XA2-15	Xa2-S	213
XA1-U	J1-TP18	27	XA2-15	S2-2	224
XA1-V	NC		XA2-16	XA2-15	214
XA1-W	NC		XA2-16	J4-TP6	112
XA1-X	NC		XA2-17	NC	
XA1-Y	NC		XA2-18	T1-8	209

Table 3-41. Test Set Subassembly MX-8638A/APS-94D, Unit 1A1, Wire List - Continued

From	To	Wire No.	From	To	Wire No.
XA2-19	NC		XA6-Y	XA2-T	191
XA2-20	L1-2	210	XA6-Z	NC	
XA2-21	NC		XA6-1	XA6-A	184
XA2-22	E-16	198	XA6-2	NC	
XA2-22	XA2-Z	196	XA6-3	NC	
XA6-A	E-15	186	XA6-4	NC	
XA6-B	NC		XA6-5	NC	
XA6-C	S1-1	188	XA6-6	NC	
XA6-D	S1-W	189	XA6-7	NC	
XA6-E	S1-2	190	XA6-8	NC	
XA6-F	NC		XA6-9	NC	
XA6-G	NC		XA6-10	NC	
XA6-H	NC		XA6-11	NC	
XA6-J	NC		XA6-12	NC	
XA6-K	NC		XA6-13	NC	
XA6-L	NC		XA6-14	NC	
XA6-M	NC		XA6-15	NC	
XA6-N	NC		XA6-16	NC	
XA6-P	NC		XA6-17	NC	
XA6-R	NC		XA6-18	NC	
XA6-S	NC		XA6-19	NC	
XA6-T	NC		XA6-20	NC	
XA6-U	XA2-E	193	XA6-21	NC	
XA6-U	J2-TP1	47	XA6-22	XA6-Z	185
XA6-V	NC		XDS1-1	PS1-1	219
XA6-W	XA2-5	192	XDS1-2	E-11	218
XA6-X	J2-TP14	54	XDS2-2	E-10	220

3-52. Test Set Subassembly MX-8638A/APD-94D, Unit 1A2 Wire List.

The wire list for unit 1A2 is presented in table 3-42. The wire list will be an aid to the repairman when testing or troubleshooting unit 1A2.

Table 3-42. Test Set Subassembly MX-8638A/APS-94D, Unit 1A2 Wire List

From—	To—	Wire No.	From—	To—	Wire No.
B1–R1	K5–B2	709A	E5	J15–TP23	683A
B1–R2	K5–A2	709B	E6	J15–TP21	682B
B1–S1	K6–B2	718A	E7	J15–TP20	682A
B1–S2	K6–A2	718B	E7	R14–CW	934
B1–S3	J18–TP3	277	E10	XA6–D	725
B1–S3	J18–TP18	718C	E11	XA6–U	726
CB1–A1	J12–B	496	E15	R6–CCW	930
CB1–A2	FL2–1	527	E15	R10–CW	932
CB2–A1	J13–A	652	E15	R18–3CW	238
CB2–A2	FL3–1	667	E15	R19–CCW	935
CB2–B1	J13–B	653	E15	TB2–7	233
CB2–B2	FL4–1	668	E17	722 SHLD	829
CB2–C1	J13–C	654	E17	722 SHLD	830
CB2–C2	FL5–1	669	E17	722 SHLD	845
CB3–A1	CB4–A1	675	E17	729 SHLD	831
CB3–A2	J11–TP50	607	E17	730 SHLD	832
CB3–B1	CB4–B1	856	E18	K4–X2	457
CB3–B2	J11–TP51	608	E18	682 SHLD	834
CB3–C1	CB4–C1	857	E18	719 SHLD	828
CB3–C2	J11–TP52	609	E18	731 SHLD	827
CB4–A1	CB3–A1	675	E23	J11–TP61	273
CB4–A1	J11–TP57	610	E25	S2–2	276
CB4–A2	K2–A2	624	E25	TB1–8	572
CB4–B1	CB3–B1	856	E25	TB2–13	378
CB4–B1	J11–TP58	611	E23	XA4–H	529
CB4–B2	K2–B2	625	FL1–1	J12–A	548
CB4–C1	CB3–C1	857	FL1–2	J22–TP2	558
CB4–C1	J11–TP59	612	FL1–2	K1–X2	456
CB4–C2	K2–C2	626	FL2–1	CB1–A2	527
E1	J15–TP24	683B	FL2–2	K1–D2	528
E2	J11–TP23	743	FL3–1	CB2–A2	667
E3	J15–TP26	683C	FL3–2	R22–1	235
E4	J15–TP22	682C	FL4–1	CB2–B2	668

Table 3-42. Test Set Subassembly MX-8638A/APS-94D, Unit 1A2 Wire List - Continued

From—	To—	Wire No.	From—	To—	Wire No.
FL4—2	R21—1	236	J10—TP10	J10—16	16
FL5—1	CB2—C2	669	J10—TP10	J17—U	713C
FL5—2	R20—1	237	J10—TP11	J10—11	413
FL6—1	J13—E	671	J10—TP11	713 SHLD	757
FL6—2	XA5—10	672	J10—TP12	J10—12	17
J1—TP1	J1—A	381	J10—TP12	J17—K	289
J1—TP1	XA6P1—A	400	J10—TP13	J10—13	18
J1—TP2	J1—B	1	J10—TP13	J25—r	315
J1—TP2	TB2—30	720	J10—TP14	J10—14	19
J1—TP3	J1—C	382	J10—TP14	J17—F	703B
J1—TP3	XA6P1—C	493	J10—TP15	J10—15	20
J1—TP4	J1—D	411	J10—TP15	J17—E	703A
J1—TP4	XA6P1—D	687	J10—TP16	J10—16	414
J1—TP5	J1—E	2	J10—TP16	703 SHLD	758
J1—TP5	TB2—21	339	J10—TP17	J10—17	21
J1—TP6	J1—F	3	J10—TP17	J17—P	704B
J1—TP6	XA6P1—F	676	J10—TP18	J10—18	22
J1—TP7	J1—G	747	J10—TP18	J17—N	704A
J1—TP8	J1—H	5	J10—TP19	J10—19	415
J1—TP8	XA6P1—H	677	J10—TP19	704 SHLD	759
J1—TP9	J1—J	6	J10—TP20	J10—20	480
J1—TP9	XA6P1—J	678	J10—TP20	J21—V	498
J1—TP10	J1—K	7	J10—TP21	J10—21	660
J1—TP10	XA6P1—K	679	J10—TP21	J21—W	561
J1—A	J1—TP1	381	J10—TP22	J10—22	481
J1—B	J1—TP2	1	J10—TP22	TB2—6	680
J1—C	J1—TP3	382	J10—TP23	J10—23	541
J1—D	J1—TP4	411	J10—TP23	TB2—8	681
J1—E	J1—TP5	2	J10—TP24	J10—24	23
J1—F	J1—TP6	3	J10—TP24	J25—G	319
J1—G	J1—TP7	747	J10—TP25	J10—25	24
J1—H	J1—TP8	5	J10—TP25	J25—E	317
J1—J	J1—TP9	6	J10—TP26	J10—26	416
J1—K	J1—TP10	7	J10—TP26	705 SHLD	760
J2	J4	844	J10—TP27	J10—27	25
J3	K4—B3	728	J10—TP27	J25—Z	705B
J4	J2	844	J10—TP28	J10—28	379
J4	XA1—4	722	J10—TP28	J25—Y	705A
J5	K4—A3	729	J10—TP29	J10—29	380
J6	XA4—3	724	J10—TP29	J25—C	316
J7	K4—A1	730	J10—TP30	J10—30	417
J8	XA1—R	719	J10—TP30	714 SHLD	761
J9	TB1—9	731	J10—TP31	J10—31	26
J10—TP1	J10—1	8	J10—TP31	J25—k	714C
J10—TP1	J17—H	637	J10—TP32	J10—32	27
J10—TP2	J10—2	9	J10—TP32	J25—A	714A
J10—TP2	J17—J	445	J10—TP33	J10—33	28
J10—TP3	J10—3	627	J10—TP33	J25—X	714B
J10—TP3	TB2—1	603	J10—TP34	J10—34	29
J10—TP4	J10—4	11	J10—TP34	J25—q	336
J10—TP4	J17—A	712A	J10—TP35	J10—35	30
J10—TP5	J10—5	12	J10—TP35	J25—s	338
J10—TP5	J17—B	712B	J10—TP36	J10—36	31
J10—TP6	J10—6	13	J10—TP36	J25—h	331
J10—TP6	J17—C	712C	J10—TP37	J10—37	32
J10—TP7	J10—7	412	J10—TP37	J25—i	332
J10—TP7	712 SHLD	756	J10—TP38	J10—38	33
J10—TP8	J10—8	14	J10—TP38	J25—j	333
J10—TP8	J17—S	713A	J10—TP39	J10—39	34
J10—TP9	J10—9	15	J10—TP39	J25—a	324
J10—TP9	J17—T	713B	J10—TP40	J10—40	35

Table 3-42. Test Set Subassembly MX-8638A/APS-94D, Unit 1A2 Wire List - Continued

From—	To—	Wire No.	From—	To—	Wire No.
J10—TP40	J25—b	325	J10—TP72	J10—72	58
J10—TP41	J10—41	36	J10—TP72	J25—H	320
J10—TP41	J25—c	326	J10—TP73	J10—73	59
J10—TP42	J10—42	37	J10—TP73	J25—L	322
J10—TP42	J25—d	327	J10—TP74	J10—74	60
J10—TP43	J10—43	38	J10—TP74	J19—F	292
J10—TP43	J25—e	328	J10—TP75	J10—75	61
J10—TP44	J10—44	39	J10—TP75	J19—D	291
J10—TP44	J25—f	329	J10—TP76	J10—76	62
J10—TP45	J10—45	40	J10—TP76	J19—B	290
J10—TP45	J25—g	330	J10—TP77	J10—77	63
J10—TP46	J10—46	41	J10—TP77	J19—N	294
J10—TP46	J25—R	691	J10—TP78	J10—78	64
J10—TP47	J10—47	542	J10—TP78	J19—P	295
J10—TP47	691 SHLD	762	J10—TP79	J10—79	65
J10—TP48	J10—48	418	J10—TP79	J19—R	296
J10—TP48	TB2—4	554	J10—TP80	J10—80	66
J10—TP49	J10—49	42	J10—TP80	J19—S	297
J10—TP49	J23—m	690	J10—TP81	J10—81	67
J10—TP50	J10—50	43	J10—TP81	J19—T	298
J10—TP50	690 SHLD	763	J10—TP82	J10—82	68
J10—TP51	J10—51	44	J10—TP82	J19—U	299
J10—TP51	TB2—6	340	J10—TP83	J10—83	69
J10—TP52	NC		J10—TP83	J19—V	300
J10—TP53	J10—53	628	J10—TP84	NC	
J10—TP53	TB2—11	604	J10—TP85	J10—85	71
J10—TP54	J10—54	629	J10—TP85	XA4—T	341
J10—TP54	TB2—9	605	J10—TP86	J10—86	72
J10—TP55	J10—55	630	J10—TP86	TP—E2	692
J10—TP55	TB2—10	606	J10—TP87	J10—87	458
J10—TP56	J10—56	543	J10—TP87	TB2—7	446
J10—TP56	TB2—12	555	J10—TP88	J10—88	419
J10—TP57	J10—57	466	J10—TP88	692 SHLD	764
J10—TP57	J25—F	471	J10—TP89	NC	
J10—TP58	J10—58	467	J10—TP90	NC	
J10—TP58	J25—J	472	J10—TP91	NC	
J10—TP59	J10—59	482	J10—TP92	NC	
J10—TP59	TB2—17	499	J10—TP93	J10—93	78
J10—TP60	J10—60	46	J10—TP93	TB2—2	342
J10—TP60	J21—P	304	J10—TP94	NC	
J10—TP61	J10—61	47	J10—TP95	NC	
J10—TP61	J21—c	310	J10—TP96	J10—96	81
J10—TP62	J10—62	48	J10—TP96	J25—p	335
J10—TP62	J21—M	302	J10—TP97	J10—97	82
J10—TP63	J10—63	49	J10—TP97	J25—m	334
J10—TP63	J21—N	303	J10—TP98	J10—98	83
J10—TP64	J10—64	50	J10—TP98	J23—i	313
J10—TP64	J21—R	305	J10—TP99	J10—99	84
J10—TP65	J10—65	51	J10—TP99	J23—j	314
J10—TP65	J21—T	307	J10—TP100	NC	
J10—TP66	J10—66	52	J10—TP101	J10—101	86
J10—TP66	J21—S	306	J10—TP101	J23—J	311
J10—TP67	J10—67	53	J10—1	J10—TP1	8
J10—TP67	J21—U	308	J10—2	J10—TP2	9
J10—TP68	NC		J10—3	J10—TP3	627
J10—TP69	J10—69	55	J10—4	J10—TP4	11
J10—TP69	J23—R	312	J10—5	J10—TP5	12
J10—TP70	J10—70	56	J10—6	J10—TP6	13
J10—TP70	J25—r	337	J10—7	J10—TP7	412
J10—TP71	J10—71	57	J10—8	J10—TP8	14
J10—TP71	J21—J	301	J10—9	J10—TP9	15

Table 3-42. Test Set Subassembly MX-8638A/APS-94D, Unit 1A2 Wire List - Continued

From—	To—	Wire No.	From—	To—	Wire No.
J10—10	J10—TP10	16	J10—71	J10—TP71	57
J10—11	J10—TP11	413	J10—72	J10—TP72	58
J10—12	J10—TP12	17	J10—73	J10—TP73	59
J10—13	J10—TP13	18	J10—74	J10—TP74	60
J10—14	J10—TP14	19	J10—75	J10—TP75	61
J10—15	J10—TP15	20	J10—76	J10—TP76	62
J10—16	J10—TP16	414	J10—77	J10—TP77	63
J10—17	J10—TP17	21	J10—78	J10—TP78	64
J10—18	J10—TP18	22	J10—79	J10—TP79	65
J10—19	J10—TP19	415	J10—80	J10—TP80	66
J10—20	J10—TP20	420	J10—81	J10—TP81	67
J10—21	J10—TP21	629	J10—82	J10—TP82	68
J10—22	J10—TP22	431	J10—83	J10—TP83	69
J10—23	J10—TP23	541	J10—84	NC	
J10—24	J10—TP24	23	J10—85	J10—TP85	71
J10—25	J10—TP25	24	J10—86	J10—TP86	72
J10—26	J10—TP26	416	J10—87	J10—TP87	458
J10—27	J10—TP27	25	J10—88	J10—TP88	419
J10—28	J10—TP28	379	J10—89	NC	
J10—29	J10—TP29	380	J10—90	NC	
J10—30	J10—TP30	417	J10—91	NC	
J10—31	J10—TP31	26	J10—92	NC	
J10—32	J10—TP32	27	J10—93	J10—TP93	76
J10—33	J10—TP33	28	J10—94	NC	
J10—34	J10—TP34	29	J10—95	NC	
J10—35	J10—TP35	30	J10—96	J10—TP96	81
J10—36	J10—TP36	31	J10—97	J10—TP97	82
J10—37	J10—TP37	32	J10—98	J10—TP98	83
J10—38	J10—TP38	33	J10—99	J10—TP99	84
J10—39	J10—TP39	34	J10—100	NC	
J10—40	J10—TP40	35	J10—101	J10—TP101	86
J10—41	J10—TP41	36	J11—TP1	J11—1	87
J10—42	J10—TP42	37	J11—TP1	XA6—1	693
J10—43	J10—TP43	38	J11—TP2	J11—2	88
J10—44	J10—TP44	39	J11—TP2	TB2—19	694
J10—45	J10—TP45	40	J11—TP3	J11—3	420
J10—46	J10—TP46	41	J11—TP3	694 SHLD	765
J10—47	J10—TP47	542	J11—TP4	J11—4	89
J10—48	J10—TP48	418	J11—TP4	L1—1	223
J10—49	J10—TP49	42	J11—TP5	J11—5	90
J10—50	J10—TP50	43	J11—TP5	L1—2	224
J10—51	J10—TP51	44	J11—TP6	NC	
J10—52	NC		J11—TP7	J11—7	91
J10—53	J10—TP53	628	J11—TP7	XA6—B	695
J10—54	J10—TP54	629	J11—TP8	J11—8	92
J10—55	J10—TP55	630	J11—TP8	TB2—20	696
J10—56	J10—TP56	543	J11—TP9	J11—9	422
J10—57	J10—TP57	466	J11—TP9	696 SHLD	766
J10—58	J10—TP58	467	J11—TP10	J11—10	93
J10—59	J10—TP59	482	J11—TP10	L2—1	225
J10—60	J10—TP60	46	J11—TP11	J11—11	94
J10—61	J10—TP61	47	J11—TP11	L2—2	226
J10—62	J10—TP62	48	J11—TP12	NC	
J10—63	J10—TP63	49	J11—TP13	J11—13	677
J10—64	J10—TP64	50	J11—TP13	TB1—1	681
J10—65	J10—TP65	51	J11—TP14	J11—14	483
J10—66	J10—TP66	52	J11—TP14	TB1—2	500
J10—67	J10—TP67	53	J11—TP15	J11—15	95
J10—68	NC		J11—TP15	XA6—L	343
J10—69	J10—TP69	55	J11—TP16	J11—16	96
J10—70	J10—TP70	56	J11—TP16	XA6—M	344

Table 3-42. Test Set Subassembly MX-8638A/APS-94D, Unit 1A2 Wire List - Continued

From—	To—	Wire No.	From—	To—	Wire No.
J11—TP17	J11—17	97	J11—TP51	CB3—B2	606
J11—TP17	XA6—K	345	J11—TP51	J11—51	591
J11—TP18	J11—18	576	J11—TP52	CB3—C2	609
J11—TP18	TB1—8	582	J11—TP52	J11—52	592
J11—TP19	NC		J11—TP53	NC	
J11—TP20	NC		J11—TP54	J11—54	488
J11—TP21	J11—21	383	J11—TP54	TB1—22	505
J11—TP21	J16—TP8	401	J11—TP55	J11—55	117
J11—TP22	J11—22	384	J11—TP55	NC	
J11—TP22	XA6—E	402	J11—TP56	NC	
J11—TP23	E2	743	J11—TP57	CB4—A1	610
J11—TP23	J11—23	100	J11—TP57	J11—57	593
J11—TP24	J11—24	424	J11—TP58	CB4—B1	611
J11—TP24	743 SHLD	769	J11—TP58	J11—58	594
J11—TP25	NC		J11—TP59	CB4—C1	612
J11—TP26	NC		J11—TP59	J11—59	595
J11—TP27	J11—27	459	J11—TP60	NC	
J11—TP27	TB1—5	447	J11—TP61	E22	273
J11—TP28	J11—28	104	J11—TP61	J11—61	560
J11—TP28	J16—TP12	346	J11—TP62	NC	
J11—TP29	J11—29	105	J11—TP63	NC	
J11—TP29	XA6—17	347	J11—TP64	J11—64	123
J11—TP30	J11—30	106	J11—TP64	K4—X1	744
J11—TP30	NC		J11—1	J11—TP1	87
J11—TP31	NC		J11—2	J11—TP2	88
J11—TP32	J11—32	108	J11—3	J11—TP3	420
J11—TP32	XA6—F	348	J11—4	J11—TP4	89
J11—TP33	J11—33	109	J11—5	J11—TP5	90
J11—TP33	NC		J11—6	NC	
J11—TP34	NC		J11—7	J11—TP7	91
J11—TP35	J11—35	111	J11—8	J11—TP8	92
J11—TP35	XA6—13	349	J11—9	J11—TP9	422
J11—TP36	J11—36	854	J11—10	J11—TP10	93
J11—TP36	NC		J11—11	J11—TP11	94
J11—TP37	J11—37	112	J11—12	NC	
J11—TP37	TB1—9	742	J11—13	J11—TP13	577
J11—TP38	J11—38	425	J11—14	J11—TP14	465
J11—TP38	742 SHLD	770	J11—15	J11—TP15	95
J11—TP39	J11—39	484	J11—16	J11—TP16	96
J11—TP39	TB1—11	501	J11—17	J11—TP17	97
J11—TP40	J11—40	485	J11—18	J11—TP18	576
J11—TP40	TB1—12	502	J11—19	NC	
J11—TP41	J11—TP42	771	J11—20	NC	
J11—TP41	J11—41	469	J11—21	J11—TP21	383
J11—TP42	J11—TP41	771	J11—22	J11—TP22	384
J11—TP42	J11—42	470	J11—23	J11—TP23	100
J11—TP43	J11—43	113	J11—24	J11—TP24	424
J11—TP43	XA4—M	741	J11—25	NC	
J11—TP44	J11—44	486	J11—26	NC	
J11—TP44	TB1—14	503	J11—27	J11—TP27	459
J11—TP45	J11—45	114	J11—28	J11—TP28	104
J11—TP46	J16—TP16	698	J11—29	J11—TP29	105
J11—TP46	J11—46	575	J11—30	J11—TP30	106
J11—TP46	J15—TP17	583	J11—31	NC	
J11—TP47	J11—47	457	J11—32	J11—TP32	108
J11—TP47	TB1—20	504	J11—33	J11—TP33	109
J11—TP48	NC		J11—34	NC	
J11—TP49	J11—49	544	J11—35	J11—TP35	111
J11—TP49	TB1—16	556	J11—36	J11—TP36	854
J11—TP50	J11—50		J11—37	J11—TP37	112
J11—TP50	CB3—A2	607	J11—38	J11—TP38	425

Table 3-42. Test Set Subassembly MX-8638A/APS-94D, Unit 1A2 Wire List - Continued

From—	To—	Wire No.	From—	To—	Wire No.
J11—39	J11—TP39	484	J15—TP1	TB1—1	484
J11—40	J11—TP40	465	J15—TP2	J15—B	499
J11—41	J11—TP41	469	J15—TP2	TB1—3	512
J11—42	J11—TP42	470	J15—TP3	J15—C	428
J11—43	J11—TP43	113	J15—TP3	J16—TP5	443
J11—44	J11—TP44	486	J15—TP4	NC	
J11—45	J11—TP45	114	J15—TP5	NC	
J11—46	J11—TP46	578	J15—TP6	J11—TP21	421
J11—47	J11—TP47	487	J15—TP6	J15—F	385
J11—48	NC		J15—TP7	NC	
J11—49	J11—TP49	544	J15—TP8	NC	
J11—50	J11—TP50		J15—TP9	NC	
J11—51	J11—TP51	[illegible]	J15—TP10	NC	
J11—52	J11—TP52	592	J15—TP11	J15—L	427
J11—53	NC		J15—TP11	TB1—5	449
J11—54	J11—TP54	486	J15—TP12	J11—TP26	346
J11—55	J11—TP55	117	J15—TP12	J15—M	130
J11—56	NC		J15—TP13	J15—N	[illegible]
J11—57	J11—TP57	593	J15—TP13	TB1—21	505
J11—58	J11—TP58	594	J15—TP14	J15—P	431
J11—59	J11—TP59	595	J15—TP14	TB1—12	507
J11—60	NC		J15—TP15	J11—TP45	[illegible]
J11—61	J11—TP61	460	J15—TP15	J15—R	131
J11—62	NC		J15—TP16	J15—S	432
J11—63	NC		J15—TP16	TB1—20	508
J11—64	J11—TP64	123	J15—TP17	J11—TP40	583
J12—A	FL1—1	543	J15—TP17	J15—T	[illegible]
J12—B	CB1—A1	498	J15—TP18	J15—U	485
J12—C	NC		J15—TP18	TB1—15	509
J13—A	CB2—A1	662	E18	888 SHLD	433
J13—B	CB2—B1	663	J15-TP19	J15—V	[illegible]
J13—C	CB2—C1	664	J15—TP19	TB1—16	567
J13—D	NC		J15—TP20	E7	432A
J13—E	FL2—1	671	J15—TP20	J15—W	132
J14—TP1	NC		J15—TP21	E8	682B
J14—TP2	NC		J15—TP21	J15—X	133
J14—TP3	J14—C	386	J15—TP22	E4	582C
J14—TP3	R15—1		J15—TP22	J15—Y	134
J14—TP4	J14—D	429	J15—TP23	E5	683A
J14—TP4	R15—2		J15—TP23	J15—Z	428
J14—TP5	NC		J15—TP24	E1	683B
J14—TP6	J14—F	156	J15—TP24	J15—a	135
J14—TP6	L3—1	229	J15—TP25	NC	
J14—TP7	NC		J15—TP26	E3	683C
J14—TP8	J14—H	158	J15—TP26	J15—c	137
J14—TP8	L4—1	230	J15—TP27	NC	
J14—TP9	J14—J	159	J15—TP28	NC	
J14—TP9	L4—2	231	J15—TP29	NC	
J14—TP10	J14—K	160	J15—TP30	NC	
J14—TP10	L3—2	232	J15—TP31	NC	
J14—A	NC		J15—TP32	NC	
J14—B	NC		J15—TP33	NC	
J14—C	J14—TP3	386	J15—TP34	NC	
J14—D	J14—TP4	429	J15—TP35	NC	
J14—E	NC		J15—TP36	NC	
J14—F	J14—TP6	156	J15—TP37	NC	
J14—G	NC		J15—TP38	NC	
J14—H	J14—TP8	158	J15—TP39	NC	
J14—J	J14—TP9	159	J15—TP40	NC	
J14—K	J14—TP10	160	J15—TP41	NC	
J15—TP1	J15—A	579	J15—A	J15—TP1	579

Table 3-42. Test Set Subassembly MX-8638A/APS-94D, Unit 1A2 Wire List - Continued

From—	To—	Wire No.
J15—B	J15—TP2	430
J15—C	J15—TP3	428
J15—D	NC	
J15—E	NC	
J15—F	J15—TP6	385
J15—G	NC	
J15—H	NC	
J15—J	NC	
J15—K	NC	
J15—L	J15—TP11	427
J15—M	J15—TP12	130
J15—N	J15—TP13	490
J15—P	J15—TP14	491
J15—R	J15—TP15	131
J15—S	J15—TP16	492
J15—T	J15—TP17	580
J15—U	J15—TP18	855
J15—V	J15—TP19	688
J15—W	J15—TP20	132
J15—X	J15—TP21	133
J15—Y	J15—TP22	134
J15—Z	J15—TP23	429
J15—a	J15—TP24	135
J15—b	NC	
J15—c	J15—TP26	137
J15—d	NC	
J15—e	NC	
J15—f	NC	
J15—g	NC	
J15—h	NC	
J15—i	NC	
J15—j	NC	
J15—k	NC	
J15—m	NC	
J15—n	NC	
J15—p	NC	
J15—q	NC	
J15—r	NC	
J15—s	NC	
J15—t	NC	
J16—TP1	J16—A	596
J16—TP1	K2—A1	613
J16—TP2	J16—B	597
J16—TP2	K2—B1	614
J16—TP3	J16—C	598
J16—TP3	K2—C1	615
J16—TP4	NC	
J16—TP5	J15—TP3	448
J16—TP5	J16—E	545
J16—TP6	NC	
J16—TP7	NC	
J16—TP8	NC	
J16—TP9	NC	
J16—TP10	J16—K	387
J16—TP10	TB2—14	403
J16—A	J16—TP1	596
J16—B	J16—TP2	597
J16—C	J16—TP3	598
J16—D	NC	
J16—E	J16—TP5	545
J16—F	NC	
J16—G	NC	
J16—H	NC	
J16—J	NC	
J16—K	J16—TP10	387
J17—A	J10—TP4	712A
J17—B	J10—TP5	712B
J17—C	J10—TP6	712C
J17—D	712 SHLD	749
J17—E	J10—TP15	703A
J17—F	J10—TP14	703B
J17—G	703 SHLD	748
J17—H	J10—TP1	637
J17—J	J10—TP2	446
J17—K	J10—TP12	239
J17—L	NC	
J17—M	NC	
J17—N	J10—TP18	704A
J17—P	J10—TP17	704B
J17—R	704 SHLD	750
J17—S	J10—TP8	713A
J17—T	J10—TP9	713B
J17—U	J10—TP10	713C
J17—V	713 SHLD	751
J18—TP1	J18—A	861
J18—TP1	K6—B1	265
J18—TP2	J18—B	862
J18—TP2	K6—A1	266
J18—TP3	B1—S3	277
J18—TP3	J18—C	863
J18—TP4	J18—D	864
J18—TP5	J18—E	865
J18—TP5	K5—A1	267
J18—TP6	J18—F	866
J18—TP6	K5—B1	268
J18—TP7	J18—G	867
J18—TP8	J18—H	631
J18—TP8	T1—5	636
J18—TP9	J18—J	430
J18—TP9	T1—6	451
J18—TP10	J18—K	173
J18—TP10	K1—D1	405
J18—TP11	NC	
J18—TP12	NC	
J18—TP13	J18—N	176
J18—TP13	K5—B3	269
J18—TP14	J18—P	177
J18—TP14	K5—A3	270
J18—TP15	J18—R	431
J18—TP15	709 SHLD	636
J18—TP16	J18—S	178
J18—TP16	K6—A3	271
J18—TP17	J18—T	179
J18—TP17	K6—B3	272
J18—TP18	B1—S3	718C
J18—TP19	J18—U	180
J18—TP19	J18—V	432
J18—TP19	718 SHLD	838
J18—A	J18—TP1	861
J18—B	J18—TP2	862
J18—C	J18—TP3	863
J18—D	J18—TP4	864

Table 3-42. Test Set Subassembly MX-8638A/APS-94D, Unit 1A2 Wire List - Continued

From—	To—	Wire No.	From—	To—	Wire No.
J18—E	J18—TP5	865	J20—J	NC	
J18—F	J18—TP6	866	J20—K	NC	
J18—G	J18—TP7	867	J20—L	J20—TP11	869
J18—H	J18—TP8	631	J20—M	J20—TP12	433
J18—J	J18—TP9	430	J20—N	J20—TP13	192
J18—K	J18—TP10	173	J20—P	J20—TP14	193
J18—L	NC		J20—R	J20—TP15	194
J18—M	NC		J20—S	J20—TP16	195
J18—N	J18—TP13	176	J20—T	J20—TP17	196
J18—P	J18—TP14	177	J20—U	J20—TP18	197
J18—R	J18—TP15	431	J20—V	J20—TP19	198
J18—S	J18—TP16	178	J21—A	NC	
J18—T	J18—TP17	179	J21—B	TB2—3	549
J18—U	J18—TP18	180	J21—C	TB2—11	599
J18—V	J18—TP19	432	J21—D	TB2—9	600
J19—A	NC		J21—E	TB2—10	601
J19—B	J10—TP76	290	J21—F	TB2—12	550
J19—C	NC		J21—G	TB2—8	497
J19—D	J10—TP75	291	J21—H	TB2—1	602
J19—E	NC		J21—J	J10—TP71	301
J19—F	J10—TP74	292	J21—K	NC	
J19—G	NC		J21—L	NC	
J19—H	NC		J21—M	J10—TP62	302
J19—J	NC		J21—N	J10—TP63	303
J19—K	NC		J21—P	J10—TP60	304
J19—L	J22—V	293	J21—R	J10—TP64	305
J19—M	TB2—3	442	J21—S	J10—TP66	306
J19—N	J10—TP77	294	J21—T	J10—TP65	307
J19—P	J10—TP78	295	J21—U	J10—TP67	308
J19—R	J10—TP79	296	J21—V	J10—TP20	498
J19—S	J10—TP80	297	J21—W	J10—TP21	551
J19—T	J10—TP81	298	J21—X	NC	
J19—U	J10—TP82	299	J21—Y	TB2—5	309
J19—V	J10—TP83	300	J21—Z	TB2—4	443
J20—TP1	J20—A	868	J21—a	NC	
J20—TP2	J20—B	182	J21—b	NC	
J20—TP3	J20—C	183	J21—c	J10—TP61	310
J20—TP4	J20—D	184	J22—TP1	NC	
J20—TP5	J20—E	185	J22—TP2	FL1—2	558
J20—TP6	J20—F	186	J22—TP2	J22—B	434
J20—TP7	NC		J22—TP3	J22—C	632
J20—TP8	NC		J22—TP3	K1—C1	616
J20—TP9	NC		J22—TP4	J22—D	633
J20—TP10	NC		J22—TP4	K1—B1	617
J20—TP11	J20—L	869	J22—TP5	J22—E	634
J20—TP12	J20—M	433	J22—TP5	K1—A1	618
J20—TP13	J20—N	192	J22—TP6	J22—F	435
J20—TP14	J20—P	193	J22—TP6	T1—1	559
J20—TP15	J20—R	194	J22—TP7	J22—G	388
J20—TP16	J20—S	195	J22—TP7	K1—D1	311
J20—TP17	J20—T	196	J22—TP8	J22—H	635
J20—TP18	J20—U	197	J22—TP8	S1—2	619
J20—TP19	J20—V	198	J22—TP9	J22—J	870
J20—A	J20—TP1	868	J22—TP10	NC	
J20—B	J20—TP2	182	J22—TP11	NC	
J20—C	J20—TP3	183	J22—TP12	J22—M	203
J20—D	J20—TP4	184	J22—TP12	TB3—E1	473
J20—E	J20—TP5	185	J22—TP13	J22—N	204
J20—F	J20—TP6	186	J22—TP13	TB3—E2	476
J20—G	NC		J22—TP14	J22—P	205
J20—H	NC		J22—TP14	TB3—E3	477

Table 3-42. Test Set Subassembly MX-8638A/APS-94D, Unit 1A2 Wire List - Continued

From—	To—	Wire No.	From—	To—	Wire No.
J22—TP15	J22—R	871	J23—W	NC	
J22—TP16	J22—S	872	J23—X	NC	
J22—TP17	J22—T	873	J23—Y	NC	
J22—TP18	J22—U	209	J23—Z	NC	
J22—TP18	TB3—E4	474	J23—a	NC	
J22—TP19	J22—V	389	J23—b	NC	
J22—TP19	K1—X1	512	J23—c	NC	
J22—TP20	J22—W	210	J23—d	NC	
J22—TP20	J26—TP9	475	J23—e	NC	
J22—TP21	J22—X	874	J23—f	NC	
J22—TP22	J22—Y	875	J23—g	NC	
J22—TP23	J22—Z	436	J23—h	NC	
J22—TP23	TB1—6	560	J23—i	J10—TP98	313
J22—TP24	J22—a	876	J23—j	J10—TP99	314
J22—TP25	J22—b	877	J23—k	NC	
J22—TP26	J22—c	878	J23—m	J10—TP49	690
J22—A	NC		J23—n	690 SHLD	752
J22—B	J22—TP2	434	J23—p	NC	
J22—C	J22—TP3	632	J23—q	NC	
J22—D	J22—TP4	633	J23—r	J10—TP13	315
J22—E	J22—TP5	634	J23—s	NC	
J22—F	J22—TP6	435	J23—t	TB2—4	562
J22—G	J22—TP7	388	J24—TP1	J24—A	880
J22—H	J22—TP8	635	J24—TP2	J24—B	881
J22—J	J22—TP9	870	J24—TP3	J24—C	882
J22—K	NC		J24—TP4	J24—D	883
J22—L	NC		J24—TP5	J24—E	884
J22—M	J22—TP12	203	J24—TP6	J24—F	496
J22—N	J22—TP13	204	J24—TP6	R1—1	
J22—P	J22—TP14	205	J24—TP7	J24—G	546
J22—R	J22—TP15	871	J24—TP7	R1—2	
J22—S	J22—TP16	872	J24—TP8	J24—H	885
J22—T	J22—TP17	873	J24—TP9	J24—J	222
J22—U	J22—TP18	209	J24—TP9	S3—3	879
J22—V	J22—TP19	389	J24—TP10	J24—K	886
J22—W	J22—TP20	210	J24—TP11	J24—L	887
J22—X	J22—TP21	874	J24—TP12	J24—M	888
J22—Y	J22—TP22	875	J24—TP13	J24—N	889
J22—Z	J22—TP23	436	J24—TP14	J24—P	890
J22—a	J22—TP24	876	J24—TP15	J24—R	228
J22—b	J22—TP25	877	J24—TP15	TB3—E7	351
J22—c	J22—TP26	878	J24—TP16	J24—S	891
J23—A	NC		J24—TP17	J24—T	892
J23—B	NC		J24—TP18	J24—U	893
J23—C	NC		J24—TP19	J24—V	894
J23—D	NC		J24—TP20	J24—W	895
J23—E	NC		J24—TP21	NC	
J23—F	NC		J24—TP22	NC	
J23—G	NC		J24—TP23	NC	
J23—H	NC		J24—TP24	J24—a	896
J23—J	J10—TP101	311	J24—TP25	J24—b	897
J23—K	NC		J24—TP26	J24—c	898
J23—L	NC		J24—TP27	NC	
J23—M	NC		J24—TP28	J24—e	899
J23—N	NC		J24—TP29	J24—f	900
J23—P	NC		J24—TP30	J24—g	242
J23—R	J10—TP69	312	J24—TP30	NC	
J23—S	NC		J24—TP31	J24—h	901
J23—T	NC		J24—TP32	J24—i	244
J23—U	NC		J24—TP32	TB3—E10	353
J23—V	J19—L	293	J24—TP33	J24—j	902

Table 3-42. Test Set Subassembly MX-8638A/APS-94D, Unit 1A2 Wire List - Continued

From—	To—	Wire No.	From—	To—	Wire No.
J24—TP33	TB3—E10	274	J25—J	J10—TP58	472
J24—TP34	NC		J25—K	NC	
J24—TP35	J24—m	903	J25—L	J10—TP73	322
J24—TP36	NC		J25—M	TB2—2	323
J24—TP36	J24—n	904	J25—N	NC	
J24—TP37	J24—p	905	J25—P	NC	
J24—TP38	J24—q	906	J25—R	J10—TP46	691
J24—TP39	J24—r	250	J25—S	691 SHLD	754
J24—TP39	84—3	264	J25—T	NC	
J24—TP40	NC		J25—U	NC	
J24—TP41	J24—t	547	J25—V	NC	
J24—TP41	TB1—7	563	J25—W	NC	
J24—A	J24—TP1	880	J25—X	J10—TP33	714B
J24—B	J24—TP2	881	J25—Y	J10—TP28	705A
J24—C	J24—TP3	882	J25—Z	J10—TP27	705B
J24—D	J24—TP4	883	J25—a	J10—TP39	324
J24—E	J24—TP5	884	J25—b	J10—TP40	325
J24—F	J24—TP6	496	J25—c	J10—TP41	326
J24—G	J24—TP7	546	J25—d	J10—TP42	327
J24—H	J24—TP8	885	J25—e	J10—TP43	328
J24—J	J24—TP9	222	J25—f	J10—TP44	329
J24—K	J24—TP10	886	J25—g	J10—TP45	330
J24—L	J24—TP11	887	J25—h	J10—TP26	331
J24—M	J24—TP12	888	J25—i	J10—TP37	332
J24—N	J24—TP13	889	J25—j	J10—TP38	333
J24—P	J24—TP14	890	J25—k	J10—TP31	714C
J24—R	J24—TP15	228	J25—m	J10—TP97	334
J24—S	J24—TP16	891	J25—n	NC	
J24—T	J24—TP17	892	J25—p	J10—TP96	335
J24—U	J24—TP18	893	J25—q	J10—TP34	336
J24—V	J24—TP19	894	J25—r	J10—TP70	337
J24—W	J24—TP20	895	J25—s	J10—TP36	338
J24—X	NC		J25—t	TB2—4	444
J24—Y	NC		J26—TP1	J26—A	907
J24—Z	NC		J26—TP2	J26—B	908
J24—a	J24—TP24	896	J26—TP3	J26—TP5	839
J24—b	J24—TP25	897	J26—TP3	J26—C	909
J24—c	J24—TP26	898	J26—TP4	J26—D	910
J24—d	NC		J26—TP5	J26—TP3	839
J24—e	J24—TP28	899	J26—TP5	J26—E	254
J24—f	J24—TP29	900	J26—TP5	TB3—E5	355
J24—g	J24—TP30	242	J26—TP6	J26—F	479
J24—h	J24—TP31	901	J26—TP6	K1—D2	514
J24—i	J24—TP32	244	J26—TP7	J26—G	253
J24—j	J24—TP33	902	J26—TP7	XA2—19	356
J24—k	NC		J26—TP8	J26—H	911
J24—m	J24—TP35	903	J26—TP9	J22—TP30	475
J24—n	J24—TP36	904	J26—TP9	J26—J	485
J24—p	J24—TP37	905	J26—TP10	J26—K	912
J24—q	J24—TP38	906	J26—TP11	J26—L	913
J24—r	J24—TP39	250	J26—TP12	J26—M	914
J24—s	NC		J26—TP13	J26—N	915
J24—t	J24—TP41	547	J26—TP14	J26—P	916
J25—A	J10—TP32	714A	J26—TP15	J26—R	254
J25—B	714 SHLD	753	J26—TP15	XA1—Y	699
J25—C	J10—TP29	318	J26—TP16	J26—S	440
J25—D	705 SHLD	755	J26—TP16	699 SHLD	840
J25—E	J10—TP25	317	J26—TP17	NC	
J25—F	J10—TP57	471	J26—TP18	NC	
J25—G	J10—TP24	319	J26—TP19	J26—V	917
J25—H	J10—TP72	320	J26—TP20	NC	

Table 3-42. Test Set Subassembly MX-8638A/APS-94D, Unit 1A2 Wire List - Continued

From—	To—	Wire No.	From—	To—	Wire No.
J26—TP21	J26—X	918	J26—i	J26—TP32	280
J26—TP22	J26—Y	919	J26—j	J26—TP33	281
J26—TP23	J26—Z	920	J26—k	J26—TP34	928
J26—TP24	J26—a	921	J26—m	J26—TP35	283
J26—TP25	J26—b	922	J26—n	J26—TP36	929
J26—TP26	J26—c	923	J26—p	J26—TP37	285
J26—TP27	J26—d	924	J26—q	J26—TP38	286
J26—TP28	J26—e	925	J26—r	J26—TP39	287
J26—TP29	J26—f	926	J26—s	J26—TP40	288
J26—TP30	J26—g	927	J26—t	J26—TP41	441
J26—TP31	J26—h	279	K1—A1	J22—TP5	618
J26—TP31	XA1—3	358	K1—A1	T1—2	623
J26—TP32	J26—i	280	K1—A1	T2—2	650
J26—TP32	XA1—D	359	K1—A2	XA6—Y	622
J26—TP33	J26—j	281	K1—B1	J22—TP4	617
J26—TP33	XA1—E	360	K1—B1	T2—3	651
J26—TP34	J26—k	928	K1—B2	XA6—T	621
J26—TP35	J26—m	283	K1—C1	J22—TP3	616
J26—TP35	XA2—17	361	K1—C1	T2—1	649
J26—TP36	J26—n	929	K1—C2	XA6—F	620
J26—TP37	J26—p	285	K1—D1	J18—TP10	406
J26—TP37	XA2—18	357	K1—D1	J22—TP7	611
J26—TP38	J26—q	286	K1—D1	XDS1—1	639
J26—TP38	XA2—21	362	K1—D2	FL2—2	526
J26—TP39	J26—r	287	K1—D2	J26—TP6	514
J26—TP39	TB3—E6	363	K1—X1	J22—TP19	512
J26—TP40	J26—s	288	K1—X2	FL1—2	455
J26—TP40	XA2—Y	364	K1—X2	XDS1—2	454
J26—TP41	J26—t	441	K2—A1	J16—TP1	613
J26—TP41	TB2—13	452	K2—A2	CB4—A2	624
J26—A	J26—TP1	907	K2—B1	J16—TP2	614
J26—B	J26—TP2	908	K2—B2	CB4—B2	625
J26—C	J26—TP3	909	K2—C1	J16—TP3	615
J26—D	J26—TP4	910	K2—C2	CB4—C2	626
J26—E	J26—TP5	264	K2—D1	K2—X2	537
J26—F	J26—TP6	479	K2—D1	K3—7	536
J26—G	J26—TP7	266	K2—D2	K3—5	533
J26—H	J26—TP8	911	K2—D3	K3—3	570
J26—J	J26—TP9	465	K2—X1	K3—2	571
J26—K	J26—TP10	912	K2—X2	K2—D1	537
J26—L	J26—TP11	913	K3—2	K2—X1	571
J26—M	J26—TP12	914	K3—2	TB1—16	576
J26—N	J26—TP13	915	K3—3	K2—D3	570
J26—P	J26—TP14	916	K3—5	K2—D2	533
J26—R	J26—TP15	264	K3—5	S5—1	534
J26—S	J26—TP16	440	K3—7	K2—D1	536
J26—T	NC		K4—A1	J7	730
J26—U	NC		K4—A1	K4—B1	825
J26—V	J26—TP19	917	K4—A3	J5	729
J26—W	NC		K4—B1	K4—A1	825
J26—X	J26—TP21	918	K4—B2	XA6—18	727
J26—Y	J26—TP22	919	K4—B3	J3	728
J26—Z	J26—TP23	920	K4—X1	J11—TP64	744
J26—a	J26—TP24	921	K4—X2	E18	457
J26—b	J26—TP25	922	K5—A1	J18—TP5	268
J26—c	J26—TP26	923	K5—A2	B1—R2	709B
J26—d	J26—TP27	924	K5—A3	J18—TP14	270
J26—e	J26—TP28	925	K5—B1	J18—TPK6	267
J26—f	J26—TP29	926	K5—B2	B1—R1	709A
J26—g	J26—TP30	927	K5—B3	J18—TP13	269
J26—h	J26—TP31	279	K5—X1	K6—X1	836

Table 3-42. Test Set Subassembly MX-8638A/APS-94D, Unit 1A2 Wire List - Continued

From—	To—	Wire No.	From—	To—	Wire No.
K5—X2	K6—X2	837	R18—3	E14	226
K6—A1	J18—TP2	266	R19—CW	E15	312
K6—A2	B1—S2	718B	R19—CCW	XA1—5	935
K6—A3	J18—TP17	272	R20—1	FL5—2	237
K6—B1	J18—TP1	265	R20—2	XA5—20	670
K6—B2	B1—S1	718A	R21—1	FL4—2	236
K6—B3	J18—TP16	271	R21—2	XA5— 5	666
K6—X1	K5—X1	836	R22—1	FL3—2	235
K6—X1	TB2—17	278	R22—2	XA5—6	665
K6—X2	K5—X2	837	S1—1	T1—3	648
L1	J11—TP4	223	S1—2	J22—TP8	619
L1	J11—TP5	224	S2—1	XDS2—1	234
L2	J11—TP10	225	S2—2	E26	276
L2	J11—TP11	228	S3—1	TB2—14	375
L3	J14—TP6	229	S3—3	J24—TP9	879
L3	J14—TP10	232	S4—1	TB1—29	531
L4	J14—TP8	230	S4—3	J24—TP34	354
L4	J14—TP9	231	S5—1	K3—5	534
NC	J10—TP62		S5—3	TB1—15	535
NC	J10—TP68		S6—2	TB3—E3	530
NC	J10—TP84		S6—3	TB1—30	376
NC	J10—TP89		S7—1	XA4—4	372
NC	J10—TP90		S7—2	TB2—7	460
NC	J10—TP91		TB1—1	J11—TP13	561
NC	J10—TP92		TB1—1	J15—TP1	564
NC	J10—TP94		TB1—1	XA6J1—9	569
NC	J10—TP96		TB1—2	J11—TP14	500
NC	J10—TP100		TB1—2	J15—TP2	510
NC	J10—62		TB1—2	XA4—5	404
NC	J10—68		TB1—2	XA6J1—J	540
NC	J10—84		TB1—3	J11—TP18	582
NC	J10—89		TB1—3	XA6J1—R	588
NC	J10—90		TB1—4	TB1—5	
NC	J10—91		TB1—4	T2—13	456
NC	J10—92		TB1—4	XA4—A	566
NC	J10—94		TB1—5	J11—TP27	447
NC	J10—96		TB1—5	J15—TP11	449
NC	J10—100		TB1—5	TB1—4	
NC	J11—TP6		TB1—5	TB1—6	
NC	J11—TP12		TB1—5	XA3—6	
NC	J11—TP19		TB1—6	J22—TP23	560
NC	J11—TP20		TB1—6	TB1—5	
NC	J11—TP25		TB1—6	TB1—7	
NC	J11—TP26		TB1—6	XA6J1—11	568
NC	J11—TP30		TB1—7	J34—TP41	562
NC	J11—TP31		TB1—7	TB1—6	
NC	J11—TP33		TB1—7	TB1—8	
NC	J11—TP34		TB1—7	TB1—27	
NC	J11—TP36		TB1—8	E25	572
NC	J11—TP48		TB1—8	TB1—7	
NC	J11—TP53		TB1—9	J9	731
NC	J11—TP56		TB1—9	J11—TP37	742
R8—CCW	E15	930	TB1—9	TB1—10	
R9—CCW	R10—CCW	931	TB1—10	TB1—9	
R10—CCW	E15	932	TB1—10	XA6—8	702
R10—CCW	R9—CCW	931	TB1—11	J11—TP39	501
R11—CCW	R14—CCW	933	TB1—11	XA6—F	523
R14—CCW	E7	934	TB1—12	J11—TP40	502
R14—CCW	R11—CCW	933	TB1—12	J15—TP14	507
R18—1	XA4—T	227	TB1—12	XA6—S	525
R18—2	XA4—W	371	TB1—13	NC	

Table 3-42. Test Set Subassembly MX-8638A/APS-94D, Unit 1A2 Wire List - Continued

From-	To-	Wire No.	From-	To-	Wire No.
XA1-A	TB2-13	563	XA2-R	NC	
XA1-A	XA1-1	843	XA2-S	XA1-L	366
XA1-B	NC		XA2-T	NC	
XA1-C	NC		XA2-U	NC	
XA1-D	J26-TP32	359	XA2-V	XA2-A	846
XA1-E	J26-TP33	360	XA2-W	NC	
XA1-F	NC		XA2-X	NC	
XA1-H	NC		XA2-Y	J26-TP40	364
XA1-J	XA1-W	841	XA2-Z	TB2-15	517
XA1-K	NC		XA2-Z	XA2-22	848
XA1-L	XA2-S	366	XA2-1	XA2-A	847
XA1-M	NC		XA2-2	NC	
XA1-N	NC		XA2-3	NC	
XA1-P	NC		XA2-4	NC	
XA1-R	J3	719	XA2-5	NC	
XA1-S	NC		XA2-6	NC	
XA1-T	XA4-16	721	XA2-7	NC	
XA1-U	XA1-20	367	XA2-8	NC	
XA1-V	NC		XA2-9	NC	
XA1-W	XA1-J	841	XA2-10	NC	
XA1-X	NC		XA2-11	NC	
XA1-Y	J26-TP15	699	XA2-12	NC	
XA1-Z	TB2-15	515	XA2-13	NC	
XA1-Z	XA1-22	516	XA2-14	NC	
XA1-1	XA1-A	843	XA2-15	NC	
XA1-2	TB2-16	585	XA2-16	NC	
XA1-3	J26-TP31	358	XA2-17	J26-TP36	361
XA1-4	J4	722	XA2-18	J26-TP37	357
XA1-5	R19-CW	318	XA2-19	J26-TP7	356
XA1-6	NC		XA2-20	TB2-16	590
XA1-7	NC		XA2-21	J26-TP38	362
XA1-8	NC		XA2-22	XA2-Z	848
XA1-9	NC		XA3-A	T2-4	639
XA1-10	NC		XA3-B	T2-5	640
XA1-11	NC		XA3-C	T2-6	641
XA1-12	NC		XA3-D	NC	
XA1-13	NC		XA3-E	TB1-29	518
XA1-14	NC		XA3-F	NC	
XA1-15	NC		XA3-H	TB2-17	519
XA1-16	NC		XA3-H	XA3-J	851
XA1-17	NC		XA3-J	XA3-H	851
XA1-18	NC		XA3-K	T2-7	642
XA1-19	NC		XA3-L	T2-8	643
XA1-20	XA1-U	367	XA3-M	T2-9	644
XA1-21	NC		XA3-N	NC	
XA1-22	XA1-Z	516	XA3-P	NC	
XA2-A	TB2-13	564	XA3-R	NC	
XA2-A	XA2-V	846	XA3-S	NC	
XA2-A	XA2-1	847	XA3-T	NC	
XA2-B	NC		XA3-U	NC	
XA2-C	NC		XA3-V	TB2-15	520
XA2-D	NC		XA3-V	XA3-W	852
XA2-E	NC		XA3-W	XA3-V	852
XA2-F	NC		XA3-X	NC	
XA2-H	NC		XA3-Y	NC	
XA2-J	NC		XA3-Z	NC	
XA2-K	NC		XA3-1	XA3-6	772
XA2-L	NC		XA3-1	XA3-16	773
XA2-M	NC		XA3-2	NC	
XA2-N	NC		XA3-3	NC	
XA2-P	NC		XA3-4	TB2-16	586

Table 3-42. Test Set Subassembly MX-8638A/APS-94D, Unit 1A2 Wire List - Continued

From—	To—	Wire No.	From—	To—	Wire No.
TB1—14	J11—TP44	503	TB2—14	XDS2—2	408
TB1—14	TB1—15		TB2—15	XA1—Z	515
TB1—14	XA6—N	524	TB2—15	XA2—Z	517
TB1—15	J15—TP18	509	TB2—15	XA3—V	520
TB1—15	S6—3	536	TB2—15	XA4—Z	522
TB1—15	TB1—14		TB2—16	XA1—2	565
TB1—16	J11—TP45	556	TB2—16	XA2—20	560
TB1—16	J15—TP19	557	TB2—16	XA3—4	566
TB1—16	K2—X1	575	TB2—16	XA4—D	567
TB1—16	TB1—17		TB2—17	J10—TP59	499
TB1—17	TB1—16		TB2—17	K6—X1	378
TB1—17	XA6—12	569	TB2—17	TB2—14	538
TB1—20	J11—TP47	504	TB2—17	XA3—H	519
TB1—20	J15—TP14	508	TB2—17	XA4—Y	521
TB1—21	J15—TP13	506	TB2—18	NC	
TB1—22	J11—TP54	505	TB2—19	J11—TP2	694
TB1—22	XA6—T	526	TB2—19	XA4—V	370
TB1—27	TB1—7		TB2—19	XA6—A	700
TB1—29	S4—1	531	TB2—20	J11—TP8	695
TB1—29	TB3—E12	532	TB2—20	XA4—N	369
TB1—29	XA3—E	518	TB2—20	XA6—2	701
TB1—30	S6—3	376	TB2—21	J1—TP5	339
TB2—1	J10—TP3	603	TB2—21	XA4—C	368
TB2—1	J21—H	602	TB2—21	XA6P1—E	746
TB2—2	J10—TP93	342	TB2—30	J1—TP2	720
TB2—2	J25—M	323	TB2—30	XA4—B	723
TB2—3	J10—TP23	681	TB2—30	XA6P2—B	777
TB2—3	J19—M	442	TB3—E1	J22—TP12	473
TB2—3	J21—B	549	TB3—E2	J22—TP13	476
TB2—4	J10—TP48	554	TB3—E2	J11—TP23	
TB2—4	J21—Z	443	TB3—E3	J22—TP14	477
TB2—4	J23—t	552	TB3—E4	J22—TP18	474
TB2—4	J26—t	444	TB3—E5	J28—TP5	355
TB2—4	TB2—7	573	TB3—E6	J28—TP39	363
TB2—5	J10—TP51	340	TB3—E7	J24—TP15	351
TB2—5	J21—Y	309	TB3—E8	S6—2	530
TB2—6	J10—TP22	680	TB3—E10	J24—TP32	363
TB2—6	J21—G	497	TB3—E10	J24—TP33	374
TB2—7	E15	233	TB3—E12	TB1—29	532
TB2—7	J10—TP87	446	TB3—E16	XDS1—1	239
TB2—7	S7—2	460	TP—E2	J10—TP86	692
TB2—7	TB2—4	573	T1—1	J22—TP6	559
TB2—7	TB2—13	574	T1—1	XA5—M	567
TB2—7	777 SHLD	536	T1—2	K1—A1	623
TB2—8	NC		T1—3	S1—1	648
TB2—9	J10—TP54	605	T1—4	XDS1—2	453
TB2—9	J21—D	600	T1—5	J18—TP8	638
TB2—10	J10—TP55	606	T1—6	J18—TP9	451
TB2—10	J21—E	601	T2—1	K1—C1	649
TB2—11	J10—TP53	604	T2—2	K1—A1	650
TB2—11	J21—C	599	T2—3	K1—B1	651
TB2—12	J10—TP56	558	T2—4	XA3—A	639
TB1—12	J21—F	550	T2—5	XA3—B	640
TB2—13	E25	378	T2—6	XA3—C	641
TB2—13	J26—TP41	452	T2—7	XA3—K	642
TB2—13	TB2—7	574	T2—8	XA3—L	643
TB2—13	XA1—A	563	T2—9	XA3—M	644
TB2—13	XA2—A	564	T2—10	XA3—20	645
TB2—14	J16—TP10	403	T2—11	XA3—21	646
TB2—14	S3—1	375	T2—12	XA3—22	647
TB2—14	TB2—17	538	T2—13	TB1—4	456

Table 3-42. Test Set Subassembly MX-8638A/APS-94D, Unit 1A2 Wire List - Continued

From—	To—	Wire No.	From—	To—	Wire No.
XA3-5	NC		XA4-17	NC	
XA3-6	XA3-1	772	XA4-18	NC	
XA3-7	NC		XA4-19	NC	
XA3-8	NC		XA4-20	NC	
XA3-9	NC		XA4-21	NC	
XA3-10	NC		XA4-22	XA4-Z	
XA3-11	NC		XA5-A	NC	
XA3-12	NC		XA5-B	XA5-C	778
XA3-13	NC		XA5-C	XA5-B	778
XA3-14	NC		XA5-C	XA5-D	779
XA3-15	NC		XA5-D	XA5-C	779
XA3-16	TB1-6	565	XA5-D	XA5-E	780
XA3-16	XA3-1	773	XA5-E	XA5-D	780
XA3-17	NC		XA5-E	XA5-2	781
XA3-18	NC		XA5-F	K1-C2	620
XA3-19	NC		XA5-F	XA5-6	797
XA3-20	T2-10	645	XA5-H	XA5-J	782
XA3-21	T2-11	646	XA5-J	XA5-H	782
XA3-22	T2-12	647	XA5-J	XA5-K	783
XA4-A	TB1-4	566	XA5-K	XA5-J	783
XA4-A	XA4-1	774	XA5-K	XA5-L	784
XA4-B	TB2-30	723	XA5-L	XA5-K	784
XA4-C	TB2-21	368	XA5-L	XA5-7	785
XA4-D	TB2-16	567	XA5-M	T1-1	667
XA4-E	NC		XA5-M	XA5-11	801
XA4-F	NC		XA5-N	XA5-P	786
XA4-H	E26	529	XA5-P	XA5-N	786
XA4-J	NC		XA5-P	XA5-R	787
XA4-K	NC		XA5-R	XA5-P	787
XA4-L	NC		XA5-R	XA5-S	788
XA4-M	J11-TP43	741	XA5-S	XA5-R	788
XA4-N	TB2-20	369	XA5-S	XA5-12	789
XA4-P	NC		XA5-T	K1-B2	621
XA4-R	NC		XA5-T	XA5-16	806
XA4-S	NC		XA5-U	XA5-V	790
XA4-T	J10-TP86	341	XA5-V	XA5-U	790
XA4-T	R18-1	227	XA5-V	XA5-W	791
XA4-U	NC		XA5-W	XA5-V	791
XA4-V	TB2-19	370	XA5-W	XA5-X	792
XA4-W	R18-2	371	XA5-X	XA5-W	792
XA4-X	XDS2-1	321	XA5-X	XA5-17	793
XA4-Y	TB2-17	521	XA5-Y	K1-A2	622
XA4-Z	TB2-15	622	XA5-Y	XA5-21	
XA4-Z	XA4-22		XA5-Z	NC	
XA4-1	XA4-A	774	XA5-1	NC	
XA4-2	721 SHLD	776	XA5-2	XA5-E	781
XA4-2	724 SHLD	775	XA5-2	XA5-3	794
XA4-3	J6	724	XA5-3	XA5-2	794
XA4-4	S7-1	372	XA5-3	XA5-4	795
XA4-5	TB1-2	404	XA5-4	XA5-3	795
XA4-6	NC		XA5-4	XA5-5	796
XA4-7	NC		XA5-5	R22-2	665
XA4-8	NC		XA5-5	XA5-4	796
XA4-9	NC		XA5-6	XA5-F	797
XA4-10	NC		XA5-7	XA5-L	785
XA4-11	NC		XA5-7	XA5-8	798
XA4-12	NC		XA5-8	XA5-7	798
XA4-13	NC		XA5-8	XA5-9	799
XA4-14	XA6-H	745	XA5-9	XA5-8	799
XA4-15	NC		XA5-9	XA5-10	800
XA4-16	XA1-T	721	XA5-10	FL6-2	672

Table 3-42. Test Set Subassembly MX-8638A/APS-94D, Unit 1A2 Wire List - Continued

From—	To—	Wire No.	From—	To—	Wire No.
XA5-10	XA5-9	800	XA6P1-B	TB2-30	777
XA5-11	XA5-M	801	XA6P1-C	J1-TP3	493
XA5-12	XA5-8	799	XA6P1-D	J1-TP4	687
XA5-12	XA5-13	802	XA6P1-E	TB2-21	746
XA5-13	XA5-12	802	XA6P1-F	J1-TP6	676
XA5-13	XA5-14	803	XA6P1-H	J1-TP8	677
XA5-14	XA5-13	803	XA6P1-J	J1-TP9	678
XA5-14	XA5-15	804	XA6P1-K	J1-TP10	679
XA5-15	R21-2	666	XDS1-1	K1-D1	539
XA5-15	XA5-14	804	XDS1-1	TB3-E16	239
XA5-16	XA5-T	805	XDS1-2	K1-X2	454
XA5-17	XA5-X	793	XDS1-2	T1-4	453
XA5-17	XA5-18	806	XDS2-1	S2-1	234
XA5-18	XA5-17	806	XDS2-1	XA4-X	321
XA5-18	XA5-19	807	XDS2-2	TB2-14	408
XA5-19	XA5-18	807	682 SHLD	E16	834
XA5-19	XA5-20	808	682 SHLD	683 SHLD	850
XA5-20	R20-2	670	683 SHLD	682 SHLD	850
XA5-20	XA5-19	808	690 SHLD	J10-TP50	763
XA5-21	XA5-Y		690 SHLD	J23-a	752
XA5-22	NC		691 SHLD	J10-TP47	762
XA6-A	TB2-19	700	691 SHLD	J25-B	754
XA6-A	XA6J1-10	373	692 SHLD	J10-TP66	764
XA6-B	J11-TP7	695	693 SHLD	XA6J1-3	814
XA6-C	NC		693 SHLD	694 SHLD	765
XA6-D	E10	725	693 SHLD	701 SHLD	812
XA6-E	J11-TP22	402	694 SHLD	J12-TP3	766
XA6-F	TB1-11	523	694 SHLD	693 SHLD	765
XA6-H	XA4-14	745	695 SHLD	696 SHLD	767
XA6-J	TB1-2	540	695 SHLD	700 SHLD	811
XA6-K	J11-TP17	345	696 SHLD	J11-TP9	766
XA6-L	J11-TP15	343	696 SHLD	695 SHLD	767
XA6-M	J11-TP16	344	698 SHLD	J16-TP18	833
XA6-N	TB1-14	524	699 SHLD	J26-TP16	840
XA6-P	J11-TP32	348	700 SHLD	XA6J1-3	813
XA6-R	TB1-3	588	700 SHLD	695 SHLD	811
XA6-S	TB1-12	525	701 SHLD	693 SHLD	812
XA6-T	TB1-22	526	702 SHLD	725 SHLD	815
XA6-U	E11	726	702 SHLD	726 SHLD	816
XA6-V	NC		703 SHLD	J10-TP16	758
XA6-1	J11-TP1	693	703 SHLD	J17-G	748
XA6-2	TB2-20	701	704 SHLD	J10-TP19	759
XA6-3	693 SHLD	814	704 SHLD	J17-R	750
XA6-3	700 SHLD	813	705 SHLD	J10-TP26	760
XA6-4	726 SHLD	817	706 SHLD	J25-D	755
XA6-5	NC		709 SHLD	J18-TP15	835
XA6-6	NC		712 SHLD	J10-TP7	756
XA6-7	NC		712 SHLD	J17-D	749
XA6-8	TB1-10	702	713 SHLD	J10-TP11	757
XA6-9	TB1-1	589	713 SHLD	J17-V	751
XA6-10	XA6J1-A	373	714 SHLD	J10-TP30	761
XA6-11	TB1-6	568	714 SHLD	J25-B	753
XA6-11	XA6J1-16	809	718 SHLD	J18-TP19	838
XA6-12	TB1-17	569	719 SHLD	E16	828
XA6-13	J11-TP35	349	721 SHLD	XA4-2	776
XA6-14	NC		722 SHLD	E17	829
XA6-15	727 SHLD	810	722 SHLD	E17	830
XA6-16	XA6J1-11	809	722 SHLD	E17	845
XA6-17	J11-TP29	347	724 SHLD	XA4-2	775
XA6-18	K4-B2	777	725 SHLD	702 SHLD	825
XA6P1-A	J1-TP1	400	726 SHLD	XA6J1-4	817

Table 3-42. Test Set Subassembly MX-8638A/APS-94D, Unit 1A2 Wire List - Continued

From—	To—	Wire No.	From—	To—	Wire No.
726 SHLD	702 SHLD	816	731 SHLD	E18	827
727 SHLD	XA6J1—16	810	742 SHLD	J11—TP38	770
729 SHLD	E17	831	743 SHLD	J11—TP24	769
730 SHLD	E17	832	777 SHLD	TB2—7	826

3-53. Test Set Subassembly MX-8639A/APS-94D, Unit 2 Wire List.

The wire list for unit 2 is presented in table 3-43. The wire list will be an aid to the repairman when testing or troubleshooting unit 2.

Table 3-43. Test Set Subassembly MX-8639A/APS-94D, Unit 2 Wire List

From—	To—	Wire No.	From—	To—	Wire No.
B1—R1	XA5—6	684A	E6	XA6—A	530
B1—R2	XA5—13	684B	E6	XA7—A	531
B1—S1	J4—TP9	699B	E7	J4—TP32	385
B1—S2	J4—TP8	399A	E7	J4—TP101	425
B2—1	S7—W6	372	E7	S7—2	795
B2—2	S7—W2	376	E8	C3 POS	572
B2—3	S7—W5	375	E8	E9	760
B2—4	S7—W4	374	E8	XA1—E	564
B2—5	B2—6	791	E8	XA2—M	565
B2—6	S15—9	477	E9	E8	760
B2—6	B2—5	791	E9	S10—3	
B1—S3	J4—TP10	699C	E9	J1—TP14	457
C1 NEG	C2 NEG	765	E9	XA3—M	566
C1 NEG	E1	432	E9	XA4—12	568
C1 NEG	J3—TP48	522	E10	C6 NEG	612
C1 POS	J3—TP46	560	E10	E11	761
C1 POS	C2 POS	770	E10	XA1—D	601
C1 POS	J5—TP3	563	E10	XA2—N	604
C2 NEG	C1 NEG	765	E11	E10	761
C2 NEG	C3 NEG	766	E11	J1—TP13	590
C2 POS	C1 POS	770	E11	J3—TP47	596
C2 POS	C3 POS	771	E11	XA3—N	605
C3 NEG	C2 NEG	766	E11	XA4—L	606
C3 NEG	C4 POS	767	E12	J1—TP50	633
C3 POS	C2 POS	771	E12	J5—TP1	639
C3 POS	E8	572	E13	J1—TP51	634
C4 NEG	C5 NEG	772	E13	J5—TP2	640
C4 NEG	J5—TP6	599	E14	J1—TP52	635
C4 POS	C3 NEG	767	E14	J5—TP3	641
C4 POS	C5 POS	768	E15	J2—TP56	520
C5 NEG	C4 NEG	772	E16	E17	762
C5 NEG	C6 NEG	773	E16	J1—TP27	413
C5 POS	C4 POS	768	E16	J2—TP43	515
C5 POS	C6 POS	769	E16	J5—TP14	523
C6 NEG	C5 NEG	773	E16	XA4—6	527
C6 NEG	E10	612	E17	E16	762
C6 POS	C5 POS	769	E17	E18	763
E1	C1 NEG	432	E17	J3—TP101	421
E1	S9A—6	533	E17	XA1—A	524
E1	S9C—11	534	E17	XA2—T	525
E3	R8—B	792	E17	XA3—T	526
E3	R6—B	428	E18	E17	763
E4	S11—7	430	E18	E33	793
E4	TB3—6	426	E18	552 SHLD	[illegible]
E5	XA5—1	528	E18	566 SHLD	719
E5	584 SHLD	749	E19	J1—TP44	554
E6	701 SHLD	751	E19	J2—TP22	557

Table 3-43. Test Set Subassembly MX-8639A/APS-94D, Unit 2 Wire List - Continued

From—	To—	Wire No.	From—	To—	Wire No.
E19	J3—TP22	558	J1—TP11	J1—11	8
E20	J1—TP37	661	J1—TP11	S3—6	673B
E20	XA4—A	660	J1—TP12	J1—12	393
E21	J1—TP47	555	J1—TP12	673 SHLD	705
E21	J3—TP26	559	J1—TP13	E11	590
E21	XA1—8	576	J1—TP13	J1—13	588
E22	XA4—2	567	J1—TP14	E9	457
E22	J1—TP45	667	J1—TP14	J1—14	458
E22	J2—TP46	652	J1—TP15	J1—15	9
E22	XA1—6	669	J1—TP15	J3—TP95	210
E22	XA4—M	661	J1—TP16	J1—16	10
E23	J2—TP49	668	J1—TP16	J3—TP96	211
E24	J1—TP48	592	J1—TP17	J1—17	11
E24	J3—TP30	594	J1—TP17	J3—TP97	212
E24	XA1—9	615	J1—TP18	E25	591
E24	XA4—1	607	J1—TP18	J1—18	681
E25	J1—TP18	591	J1—TP19	NC	
E25	J3—TP13	593	J1—TP20	NC	
E25	J5—TP10	600	J1—TP21	J1—21	451
E26	J1—TP49	617	J1—TP21	J5—TP17	456
E26	J2—TP23	618	J1—TP22	J1—22	452
E26	J3—TP23	621	J1—TP22	J5—TP18	459
E28	XDS1—2	359	J1—TP23	J1—23	14
E29	XDS2—2	360	J1—TP23	XA4—C	650
E31	S10—2	463	J1—TP24	J1—24	394
E32	XDS3—2	361	J1—TP24	660 SHLD	706
E33	E18	793	J1—TP24	674 SHLD	707
E33	660 SHLD	744	J1—TP25	NC	
E33	661 SHLD	742	J1—TP26	NC	
E33	667 SHLD	709	J1—TP27	E16	418
E33	669 SHLD	832	J1—TP27	J1—27	17
E37	J4—TP46	466	J1—TP28	J1—28	18
E37	S10—3	573	J1—TP28	J3—TP60	213
E37	XA1—C	386	J1—TP29	J1—29	19
E38	S7—1	389	J1—TP29	J3—TP54	674A
E39	J1—TP54	666	J1—TP30	J1—30	20
E39	J2—TP59	545	J1—TP30	J3—TP55	674B
E7	J1—TP42	501	J1—TP31	NC	
E7	J2—TP68	507	J1—TP32	J1—32	22
J1—TP1	J1—1	1	J1—TP32	J2—TP96	214
J1—TP1	S3—1	670A	J1—TP33	J1—33	23
J1—TP2	J1—TP6	710	J1—TP33	J2—TP97	215
J1—TP2	J1—2	2	J1—TP34	NC	
J1—TP2	S3—3	670B	J1—TP35	J1—35	25
J1—TP3	J1—3	390	J1—TP35	J2—TP98	216
J1—TP3	670 SHLD	702	J1—TP36	J1—36	26
J1—TP4	J1—4	3	J1—TP36	J2—TP99	217
J1—TP4	S3—4	671A	J1—TP37	E20	661
J1—TP5	J1—TP2	710	J1—TP37	J1—37	27
J1—TP6	J1—5	4	J1—TP38	J1—38	395
J1—TP6	S3—2	671B	J1—TP38	661 SHLD	708
J1—TP6	J1—6	391	J1—TP39	J1—39	540
J1—TP6	671 SHLD	703	J1—TP39	J5—TP11	552
J1—TP7	J1—7	5	J1—TP40	J1—40	541
J1—TP7	S3—5	672A	J1—TP40	J5—TP12	553
J1—TP8	J1—8	6	J1—TP41	J1—41	490
J1—TP8	S3—7	672B	J1—TP41	J2—TP57	502
J1—TP9	J1—9	392	J1—TP42	E7	501
J1—TP9	672 SHLD	704	J1—TP42	J1—42	491
J1—TP10	J1—10	7	J1—TP43	J1—43	28
J1—TP10	S3—8	673A	J1—TP43	J2—TP49	218

Table 3-43. Test Set Subassembly MX-8639A/APS-94D, Unit 2 Wire List - Continued

From—	To—	Wire No.	From—	To—	Wire No.
J1—TP44	E19	554	J1—26	NC	
J1—TP44	J1—44	542	J1—27	J1—TP27	17
J1—TP45	E22	667	J1—28	J1—TP28	18
J1—TP45	J1—45	29	J1—29	J1—TP29	19
J1—TP46	E24	582	J1—30	J1—TP30	20
J1—TP46	J1—46	582	J1—31	NC	
J1—TP47	E21	555	J1—32	J1—TP32	22
J1—TP47	J1—47	543	J1—33	J1—TP33	23
J1—TP48	NC		J1—34	NC	
J1—TP49	E26	517	J1—35	J1—TP35	25
J1—TP49	J1—49	510	J1—36	J1—TP36	26
J1—TP50	E12	633	J1—37	J1—TP37	27
J1—TP50	J1—50	620	J1—38	J1—TP38	395
J1—TP51	E13	634	J1—39	J1—TP39	540
J1—TP51	J1—51	621	J1—40	J1—TP40	541
J1—TP52	E14	635	J1—41	J1—TP41	490
J1—TP52	J1—52	622	J1—42	J1—TP42	491
J1—TP53	NC		J1—43	J1—TP43	28
J1—TP54	E30	566	J1—44	J1—TP44	542
J1—TP54	J1—54	544	J1—45	J1—TP45	29
J1—TP55	J1—55	30	J1—46	J1—TP46	582
J1—TP55	J3—TP60	220	J1—47	J1—TP47	543
J1—TP56	NC		J1—48	NC	
J1—TP57	J1—57	623	J1—49	J1—TP49	510
J1—TP57	J2—TP53	636	J1—50	J1—TP50	620
J1—TP58	J1—58	624	J1—51	J1—TP51	621
J1—TP58	J2—TP54	637	J1—52	J1—TP52	622
J1—TP59	J1—59	625	J1—53	NC	
J1—TP59	J2—TP55	638	J1—54	J1—TP54	544
J1—TP60	NC		J1—55	J1—TP55	30
J1—TP61	J1—61	12	J1—56	NC	
J1—TP61	S7—W1	396	J1—57	J1—TP57	623
J1—TP62	NC		J1—58	J1—TP58	624
J1—TP63	NC		J1—59	J1—TP59	625
J1—TP64	J1—64	31	J1—60	NC	
J1—TP64	J2—TP101	221	J1—61	J1—TP61	12
J1—1	J1—TP1	1	J1—62	NC	
J1—2	J1—TP2	2	J1—63	NC	
J1—3	J1—TP3	390	J1—64	J1—TP64	31
J1—4	J1—TP4	3	J2—TP1	J2—1	[illegible]
J1—5	J1—TP5	4	J2—TP1	J3—TP1	[illegible]
J1—6	J1—TP6	391	J2—TP2	J2—2	396
J1—7	J1—TP7	5	J2—TP2	J3—TP2	412
J1—8	J1—TP8	6	J2—TP3	J2—3	626
J1—9	J1—TP9	392	J2—TP3	J3—TP3	436
J1—10	J1—TP10	7	J2—TP4	J2—4	32
J1—11	J1—TP11	8	J2—TP4	J3—TP4	696A
J1—12	J1—TP12	393	J2—TP5	J2—5	33
J1—13	J1—TP13	580	J2—TP5	J3—TP5	696B
J1—14	J1—TP14	450	* J2—TP6	J2—6	34
J1—15	J1—TP15	9	J2—TP6	J3—TP6	696C
J1—16	J1—TP16	10	J2—TP7	J2—7	397
J1—17	J1—TP17	11	J2—TP7	696 SHLD	
J1—18	J1—TP18	581	J2—TP8	J2—8	35
J1—19	NC		J2—TP8	J3—TP8	696A
J1—20	NC		J2—TP9	J2—9	36
J1—21	J1—TP21	451	J2—TP9	J3—TP9	696B
J1—22	J1—TP22	452	J2—TP10	J2—10	37
J1—23	J1—TP23	14	J2—TP10	J3—TP10	696C
J1—24	J1—TP24	394	J2—TP11	J2—11	398
J1—25	NC		J2—TP11	696 SHLD	711

Table 3-43. Test Set Subassembly MX-8639A/APS-94D, Unit 2 Wire List - Continued

From—	To—	Wire No.	From—	To—	Wire No.
J2—TP12	J2—12	38	J2—TP42	J3—TP42	238
J2—TP12	J3—TP12	222	J2—TP43	J2—43	63
J2—TP13	J2—13	39	J2—TP43	J3—TP43	239
J2—TP13	XA4—N	223	J2—TP44	J2—44	64
J2—TP14	J2—14	40	J2—TP44	J3—TP44	240
J2—TP14	J3—TP14	675A	J2—TP45	J2—45	65
J2—TP15	J2—15	41	J2—TP45	J3—TP45	241
J2—TP15	J3—TP15	675B	J2—TP46	E22	552
J2—TP16	J2—16	399	J2—TP46	J2—46	66
J2—TP16	675 SHLD	712	J2—TP47	J2—47	404
J2—TP17	J2—17	42	J2—TP47	652 SHLD	716
J2—TP17	J3—TP17	676A	J2—TP48	E16	519
J2—TP18	J2—18	43	J2—TP48	J2—48	511
J2—TP18	J3—TP18	676B	J2—TP49	E23	556
J2—TP19	J2—19	400	J2—TP49	J2—49	67
J2—TP19	676 SHLD	713	J2—TP50	J2—50	405
J2—TP20	J2—20	44	J2—TP50	668 SHLD	718
J2—TP20	J3—TP20	502	J2—TP51	J2—51	68
J2—TP21	J2—21	45	J2—TP51	J3—TP51	243
J2—TP21	J3—TP21	503	J2—TP52	NC	
J2—TP22	E19	557	J2—TP53	J1—TP57	626
J2—TP22	J2—22	453	J2—TP53	J2—53	627
J2—TP23	E26	518	J2—TP54	J1—TP58	637
J2—TP23	J2—23	401	J2—TP54	J2—54	625
J2—TP24	J2—24	46	J2—TP55	J1—TP60	638
J2—TP24	J3—TP24	224	J2—TP55	J2—55	629
J2—TP25	J2—25	47	J2—TP56	E16	530
J2—TP25	J3—TP25	225	J2—TP56	J2—56	512
J2—TP26	J2—26	402	J2—TP57	J1—TP41	500
J2—TP26	677 SHLD	714	J2—TP57	J2—57	492
J2—TP27	J2—27	48	J2—TP58	E7	507
J2—TP27	J3—TP27	677A	J2—TP58	J2—58	493
J2—TP28	J2—28	49	J2—TP59	E39	545
J2—TP28	J3—TP28	677B	J2—TP60	J2—60	69
J2—TP29	J2—29	50	J2—TP60	J3—TP60	244
J2—TP29	J3—TP29	226	J2—TP61	J2—61	70
J2—TP30	J2—30	403	J2—TP61	J3—TP61	245
J2—TP30	697 SHLD	715	J2—TP62	J2—62	71
J2—TP31	J2—31	51	J2—TP62	J3—TP62	246
J2—TP31	J3—TP31	697A	J2—TP63	J2—63	72
J2—TP32	J2—32	52	J2—TP63	J3—TP63	247
J2—TP32	J3—TP32	697B	J2—TP64	J2—64	73
J2—TP33	J2—33	53	J2—TP64	J3—TP64	248
J2—TP33	J3—TP33	697C	J2—TP65	J2—65	74
J2—TP34	J2—34	54	J2—TP65	J3—TP65	249
J2—TP34	J3—TP34	230	J2—TP66	J2—66	75
J2—TP35	J2—35	55	J2—TP66	J3—TP66	250
J2—TP35	J3—TP35	231	J2—TP67	J2—67	76
J2—TP36	J2—36	56	J2—TP67	J3—TP67	251
J2—TP36	J3—TP36	232	J2—TP68	NC	
J2—TP37	J2—37	57	J2—TP69	J2—69	77
J2—TP37	J3—TP37	233	J2—TP69	J3—TP69	252
J2—TP38	J2—38	58	J2—TP70	J2—70	78
J2—TP38	J3—TP38	234	J2—TP70	J3—TP70	253
J2—TP39	J2—39	59	J2—TP71	J2—71	79
J2—TP39	J3—TP39	235	J2—TP71	J3—TP71	254
J2—TP40	J2—40	60	J2—TP72	J2—72	80
J2—TP40	J3—TP40	236	J2—TP72	J3—TP72	255
J2—TP41	J2—41	61	J2—TP73	J2—73	81
J2—TP41	J3—TP41	237	J2—TP73	J3—TP73	256
J2—TP42	J2—42	62	J2—TP74	J2—74	82

Table 3-43. Test Set Subassembly MX-8639A/APS-94D, Unit 2 Wire List - Continued

From—	To—	Wire No.	From—	To—	Wire No.
J2—TP74	J3—TP74	257	J2—14	J2—TP14	40
J2—TP75	J2—75	83	J2—15	J2—TP15	41
J2—TP75	J3—TP75	258	J2—16	J2—TP16	399
J2—TP76	J2—76	84	J2—17	J2—TP17	42
J2—TP76	J3—TP76	259	J2—18	J2—TP18	43
J2—TP77	J2—77	85	J2—19	J2—TP19	400
J2—TP77	J3—TP77	260	J2—20	J2—TP20	44
J2—TP78	J2—78	86	J2—21	J2—TP21	45
J2—TP78	J3—TP78	261	J2—22	J2—TP22	453
J2—TP79	J2—79	87	J2—23	J2—TP23	401
J2—TP79	J3—TP79	262	J2—24	J2—TP24	46
J2—TP80	J2—80	88	J2—25	J2—TP25	47
J2—TP80	J3—TP80	263	J2—26	J2—TP26	402
J2—TP81	J2—81	89	J2—27	J2—TP27	48
J2—TP81	J3—TP81	264	J2—28	J2—TP28	49
J2—TP82	J2—82	90	J2—29	J2—TP29	50
J2—TP82	J3—TP82	265	J2—30	J2—TP30	403
J2—TP83	J2—83	91	J2—31	J2—TP31	51
J2—TP83	J3—TP83	266	J2—32	J2—TP32	52
J2—TP84	NC		J2—33	J2—TP33	53
J2—TP85	J2—85	92	J2—34	J2—TP34	54
J2—TP85	J3—TP85	698A	J2—35	J2—TP35	55
J2—TP86	J2—86	93	J2—36	J2—TP36	56
J2—TP86	J3—TP86	698B	J2—37	J2—TP37	57
J2—TP87	J2—87	94	J2—38	J2—TP38	58
J2—TP87	J3—TP87	698C	J2—39	J2—TP39	59
J2—TP88	J2—88	407	J2—40	J2—TP40	60
J2—TP88	698 SHLD	720	J2—41	J2—TP41	61
J2—TP89	NC		J2—42	J2—TP42	62
J2—TP90	NC		J2—43	J2—TP43	63
J2—TP91	NC		J2—44	J2—TP44	64
J2—TP92	NC		J2—45	J2—TP45	65
J2—TP93	J2—93	95	J2—46	J2—TP46	66
J2—TP93	J3—TP93	267	J2—47	J2—TP47	404
J2—TP94	J2—94	96	J2—48	J2—TP48	511
J2—TP94	J3—TP94	268	J2—49	J2—TP49	67
J2—TP95	NC		J2—50	J2—TP50	405
J2—TP96	J1—TP32	214	J2—51	J2—TP51	68
J2—TP96	J2—96	97	J2—52	NC	
J2—TP97	J1—TP33	215	J2—53	J2—TP53	627
J2—TP97	J2—97	98	J2—54	J2—TP54	628
J2—TP98	J1—TP35	216	J2—55	J2—TP55	629
J2—TP98	J2—98	99	J2—56	J2—TP56	512
J2—TP99	J1—TP36	217	J2—57	J2—TP57	492
J2—TP99	J2—99	100	J2—58	J2—TP58	493
J2—TP100	NC		J2—60	J2—TP60	69
J2—TP101	J1—TP64	221	J2—61	J2—TP61	70
J2—TP101	J2—101	101	J2—62	J2—TP62	71
J2—1	J2—TP1	480	J2—63	J2—TP63	72
J2—2	J2—TP2	396	J2—64	J2—TP64	73
J2—3	J2—TP3	626	J2—65	J2—TP65	74
J2—4	J2—TP4	32	J2—66	J2—TP66	75
J2—5	J2—TP5	33	J2—67	J2—TP67	76
J2—6	J2—TP6	34	J2—68	NC	
J2—7	J2—TP7	397	J2—69	J2—TP69	77
J2—8	J2—TP8	35	J2—70	J2—TP70	78
J2—9	J2—TP9	36	J2—71	J2—TP71	79
J2—10	J2—TP10	37	J2—72	J2—TP72	80
J2—11	J2—TP11	398	J2—73	J2—TP73	81
J2—12	J2—TP12	38	J2—74	J2—TP74	82
J2—13	J2—TP13	39	J2—75	J2—TP75	83

Table 3-43. Test Set Subassembly MX-8639A/APS-94D, Unit 2 Wire List - Continued

From—	To—	Wire No.	From—	To—	Wire No.
J2—76	J2—TP76	84	J3—TP18	J3—18	111
J2—77	J2—TP77	85	J3—TP19	J3—19	412
J2—78	J2—TP78	86	J3—TP19	676 SHLD	831
J2—79	J2—TP79	87	J3—TP20	J2—TP20	502
J2—80	J2—TP80	88	J3—TP20	J3—20	495
J2—81	J2—TP81	89	J3—TP21	J2—TP21	503
J2—82	J2—TP82	90	J3—TP21	J3—21	496
J2—83	J2—TP83	91	J3—22	E19	556
J2—84	NC		J3—TP22	J3—22	546
J2—85	J2—TP85	92	J3—TP23	E26	521
J2—86	J2—TP86	93	J3—TP23	J3—23	513
J2—87	J2—TP87	94	J3—TP24	J2—TP24	224
J2—88	J2—TP88	407	J3—TP24	J3—24	112
J2—89	NC		J3—TP25	J2—TP25	225
J2—90	NC		J3—TP25	J3—25	113
J2—91	NC		J3—TP26	E21	558
J2—92	NC		J3—TP26	J3—26	547
J2—93	J2—TP93	95	J3—TP27	J2—TP27	677A
J2—94	J2—TP94	96	J3—TP27	J3—27	114
J2—95	NC		J3—TP28	J2—TP28	677B
J2—96	J2—TP96	97	J3—TP28	J3—28	115
J2—97	J2—TP97	98	J3—TP29	J2—TP29	226
J2—98	J2—TP98	99	J3—TP29	J3—29	116
J2—99	J2—TP99	100	J3—TP30	E24	594
J2—100	NC		J3—TP30	J3—30	614
J2—101	J2—TP101	101	J3—TP31	J2—TP31	697A
J3—TP1	J2—TP1	484	J3—TP31	J3—31	117
J3—TP1	J3—1	481	J3—TP32	J2—TP32	697B
J3—TP2	J2—TP2	419	J3—TP32	J3—32	118
J3—TP2	J3—2	408	J3—TP33	J2—TP33	697C
J3—TP3	J2—TP3	485	J3—TP33	J3—33	119
J3—TP3	J3—3	482	J3—TP34	J2—TP34	230
J3—TP4	J2—TP4	695A	J3—TP34	J3—34	120
J3—TP4	J3—4	102	J3—TP35	J2—TP35	231
J3—TP5	J2—TP5	695B	J3—TP35	J3—35	121
J3—TP5	J3—5	103	J3—TP36	J2—TP36	232
J3—TP6	J2—TP6	695C	J3—TP36	J3—36	122
J3—TP6	J3—6	104	J3—TP37	J2—TP37	233
J3—TP7	J3—7	409	J3—TP37	J3—37	123
J3—TP7	695 SHLD	828	J3—TP38	J2—TP38	234
J3—TP8	J2—TP8	696A	J3—TP38	J3—38	124
J3—TP8	J3—8	105	J3—TP39	J2—TP39	235
J3—TP9	J2—TP9	696B	J3—TP39	J3—39	125
J3—TP9	J3—9	106	J3—TP40	J2—TP40	236
J3—TP10	J2—TP10	696C	J3—TP40	J3—40	126
J3—TP10	J3—10	107	J3—TP41	J2—TP41	237
J3—TP11	J3—11	410	J3—TP41	J3—41	127
J3—TP11	696 SHLD	829	J3—TP42	J2—TP42	238
J3—TP12	J2—TP12	222	J3—TP42	J3—42	128
J3—TP12	J3—12	494	J3—TP43	J2—TP43	239
J3—TP13	E25	593	J3—TP43	J3—43	129
J3—TP13	J3—13	583	J3—TP44	J2—TP44	240
J3—TP14	J2—TP14	675A	J3—TP44	J3—44	130
J3—TP14	J3—14	108	J3—TP45	J2—TP45	241
J3—TP15	J2—TP15	675B	J3—TP45	J3—45	131
J3—TP15	J3—15	109	J3—TP46	C1 POS	560
J3—TP16	J3—16	411	J3—TP46	J3—46	548
J3—TP16	675 SHLD	830	J3—TP47	E11	595
J3—TP17	J2—TP17	676A	J3—TP47	J3—47	584
J3—TP17	J3—17	110	J3—TP48	C1 NEG	522
J3—TP18	J2—TP18	676B	J3—TP48	J3—48	614

Table 3-43. Test Set Subassembly MX-8639A/APS-94D, Unit 2 Wire List - Continued

From—	To—	Wire No.	From—	To—	Wire No.
J3—TP49	J1—TP43	218	J3—TP79	J3—79	162
J3—TP49	J3—49	132	J3—TP80	J2—TP80	263
J3—TP50	J1—TP28	213	J3—TP80	J3—80	163
J3—TP50	J3—50	133	J3—TP81	J2—TP81	264
J3—TP51	J2—TP51	243	J3—TP81	J3—81	164
J3—TP51	J3—51	134	J3—TP82	J2—TP82	265
J3—TP52	J3—52	135	J3—TP82	J3—82	165
J3—TP52	XA4—R	678B	J3—TP83	J2—TP83	266
J3—TP53	J3—53	136	J3—TP83	J3—83	166
J3—TP53	XA4—P	678A	J3—TP84	J3—84	167
J3—TP54	J1—TP29	674A	J3—TP84	XA4—13	655
J3—TP54	J3—54	137	J3—TP85	J2—TP85	698A
J3—TP55	J1—TP30	674B	J3—TP85	J3—85	168
J3—TP55	J3—55	138	J3—TP86	J2—TP86	698B
J3—TP56	J3—56	139	J3—TP86	J3—86	169
J3—TP56	XA4—15	679A	J3—TP87	J2—TP87	698C
J3—TP57	J3—57	140	J3—TP87	J3—87	170
J3—TP57	XA4—14	679B	J3—TP88	J3—88	413
J3—TP58	J3—58	141	J3—TP88	698 SHLD	
J3—TP58	XA4—E	653	J3—TP89	NC	
J3—TP59	J3—59	142	J3—TP90	NC	
J3—TP59	XA4—D	654	J3—TP91	NC	
J3—TP60	J2—TP60	244	J3—TP92	NC	
J3—TP60	J3—60	143	J3—TP93	J2—TP93	267
J3—TP61	J2—TP61	245	J3—TP93	J3—93	171
J3—TP61	J3—61	144	J3—TP94	J2—TP94	268
J3—TP62	J2—TP62	246	J3—TP94	J3—94	172
J3—TP62	J3—62	145	J3—TP95	J1—TP15	210
J3—TP63	J2—TP63	247	J3—TP95	J3—95	173
J3—TP63	J3—63	146	J3—TP96	J1—TP16	211
J3—TP64	J2—TP64	248	J3—TP96	J3—96	174
J3—TP64	J3—64	147	J3—TP97	J1—TP17	212
J3—TP65	J2—TP65	249	J3—TP97	J3—97	175
J3—TP65	J3—65	148	J3—TP98	NC	
J3—TP66	J2—TP66	250	J3—TP99	NC	
J3—TP66	J3—66	149	J3—TP100	NC	
J3—TP67	J2—TP67	251	J3—TP101	E17	421
J3—TP67	J3—67	150	J3—TP101	J3—101	176
J3—TP68	J1—TP55	220	J3—1	J3—TP1	481
J3—TP68	J3—68	151	J3—2	J3—TP2	408
J3—TP69	J2—TP69	252	J3—3	J3—TP3	482
J3—TP69	J3—69	152	J3—4	J3—TP4	102
J3—TP70	J2—TP70	253	J3—5	J3—TP5	103
J3—TP70	J3—70	153	J3—6	J3—TP6	104
J3—TP71	J2—TP71	254	J3—7	J3—TP7	409
J3—TP71	J3—71	154	J3—8	J3—TP8	105
J3—TP72	J2—TP72	255	J3—9	J3—TP9	106
J3—TP72	J3—72	155	J3—10	J3—TP10	107
J3—TP73	J2—TP73	256	J3—11	J3—TP11	410
J3—TP73	J3—73	156	J3—12	J3—TP12	494
J3—TP74	J2—TP74	257	J3—13	J3—TP13	583
J3—TP74	J3—74	157	J3—14	J3—TP14	108
J3—TP75	J2—TP75	258	J3—15	J3—TP15	109
J3—TP75	J3—75	158	J3—16	J3—TP16	411
J3—TP76	J2—TP76	259	J3—17	J3—TP17	110
J3—TP76	J3—76	159	J3—18	J3—TP18	111
J3—TP77	J2—TP77	260	J3—19	J3—TP19	412
J3—TP77	J3—77	160	J3—20	J3—TP20	495
J3—TP78	J2—TP78	261	J3—21	J3—TP21	496
J3—TP78	J3—78	161	J3—22	J3—TP22	546
J3—TP79	J2—TP79	262	J3—23	J3—TP23	513

Table 3-43. Test Set Subassembly MX-8639A/APS-94D, Unit 2 Wire List - Continued

From—	To—	Wire No.	From—	To—	Wire No.
J3—24	J3—TP24	112	J3—85	J3—TP85	168
J3—25	J3—TP25	113	J3—86	J3—TP86	169
J3—26	J3—TP26	547	J3—87	J3—TP87	170
J3—27	J3—TP27	114	J3—88	J3—TP88	415
J3—28	J3—TP28	115	J3—89	NC	
J3—29	J3—TP29	116	J3—90	NC	
J3—30	J3—TP30	614	J3—91	NC	
J3—31	J3—TP31	117	J3—92	NC	
J3—32	J3—TP32	118	J3—93	J3—TP93	171
J3—33	J3—TP33	119	J3—94	J3—TP94	172
J3—34	J3—TP34	120	J3—95	J3—TP95	173
J3—35	J3—TP35	121	J3—96	J3—TP96	174
J3—36	J3—TP36	122	J3—97	J3—TP97	175
J3—37	J3—TP37	123	J3—98	NC	
J3—38	J3—TP38	124	J3—99	NC	
J3—39	J3—TP39	125	J3—100	NC	
J3—40	J3—TP40	126	J3—101	J3—TP101	176
J3—41	J3—TP41	127	J4—TP1	J4—1	483
J3—42	J3—TP42	128	J4—TP1	XA5—5	486
J3—43	J3—TP43	129	J4—TP2	J4—2	414
J3—44	J3—TP44	130	J4—TP2	XA5—13	422
J3—45	J3—TP45	131	J4—TP3	J4—3	837
J3—46	J3—TP46	548	J4—TP4	J4—TP8	721
J3—47	J3—TP47	584	J4—TP4	J4—4	838
J3—48	J3—TP48	514	J4—TP5	J4—TP9	722
J3—49	J3—TP49	132	J4—TP5	J4—5	839
J3—50	J3—TP50	133	J4—TP6	J4—TP10	723
J3—51	J3—TP51	134	J4—TP6	J4—6	840
J3—52	J3—TP52	135	J4—TP7	J4—TP11	724
J3—53	J3—TP53	136	J4—TP7	J4—7	851
J3—54	J3—TP54	137	J4—TP8	B1—S2	699A
J3—55	J3—TP55	138	J4—TP8	J4—TP4	721
J3—56	J3—TP56	139	J4—TP8	J4—8	177
J3—57	J3—TP57	140	J4—TP8	F —S1	699B
J3—58	J3—TP58	141	J4—TP9	J4—TP5	722
J3—59	J3—TP59	142	J4—TP9	B2—S2	
J3—60	J3—TP60	143	J4—TP9	J4—9	178
J3—61	J3—TP61	144	J4—TP10	B2—S3	699C
J3—62	J3—TP62	145	J4—TP10	J4—TP6	723
J3—63	J3—TP63	146	J4—TP10	J4—10	179
J3—64	J3—TP64	147	J4—TP11	J4—TP7	724
J3—65	J3—TP65	148	J4—TP11	J4—11	415
J3—66	J3—TP66	149	J4—TP11	699 SHLD	725
J3—67	J3—TP67	150	J4—TP12	J4—12	497
J3—68	J3—TP68	151	J4—TP12	XA5—9	504
J3—69	J3—TP69	152	J4—TP13	J4—13	585
J3—70	J3—TP70	153	J4—TP13	XA1—21	603
J3—71	J3—TP71	154	J4—TP13	XA6—W	593
J3—72	J3—TP72	155	J4—TP14	J4—14	842
J3—73	J3—TP73	156	J4—TP14	XA5—12	382
J3—74	J3—TP74	157	J4—TP15	J4—15	843
J3—75	J3—TP75	158	J4—TP15	XA5—3	332
J3—76	J3—TP76	159	J4—TP16	J4—16	844
J3—77	J3—TP77	160	J4—TP17	J4—17	180
J3—78	J3—TP78	161	J4—TP17	XA5—14	269
J3—79	J3—TP79	162	J4—TP18	J4—18	181
J3—80	J3—TP80	163	J4—TP18	XA5—11	335
J3—81	J3—TP81	164	J4—TP19	J4—19	845
J3—82	J3—TP82	165	J4—TP20	J4—20	498
J3—83	J3—TP83	166	J4—TP20	S5—3	505
J3—84	J3—TP84	167	J4—TP21	J4—21	499

Table 3-43. Test Set Subassembly MX-8639A/APS-94D, Unit 2 Wire List - Continued

From—	To—	Wire No.	From—	To—	Wire No.
J4—TP21	S5—2	506	J4—TP58	J4—58	197
J4—TP22	J4—22	846	J4—TP58	XA6—R	286
J4—TP23	J4—23	416	J4—TP59	J4—59	198
J4—TP23	XA5—K	425	J4—TP59	XA6—H	287
J4—TP24	J4—24	182	J4—TP60	J4—60	199
J4—TP24	XA1—10	271	J4—TP60	XA7—3	526
J4—TP25	J4—25	183	J4—TP61	J4—61	850
J4—TP25	XA7—5	272	J4—TP62	J4—62	861
J4—TP26	J4—26	549	J4—TP63	J4—63	862
J4—TP26	XA6—V	561	J4—TP64	J4—64	863
J4—TP27	J4—27	847	J4—TP65	J4—65	864
J4—TP28	J4—28	848	J4—TP66	J4—66	865
J4—TP29	J4—29	13	J4—TP67	J4—67	200
J4—TP30	J4—30	586	J4—TP67	XA7—4	289
J4—TP30	XA6—X	597	J4—TP68	J4—68	201
J4—TP31	J4—31	849	J4—TP68	S9A—W2	290
J4—TP32	E7	365	J4—TP69	J4—69	203
J4—TP32	J4—32	850	J4—TP69	XA7—9	291
J4—TP33	J4—33	851	J4—TP70	J4—70	204
J4—TP34	J4—34	184	J4—TP70	XA7—2	292
J4—TP34	S9C—1	273	J4—TP71	J4—71	866
J4—TP35	J4—35	185	J4—TP72	J4—72	867
J4—TP35	S9C—3	274	J4—TP73	J4—73	868
J4—TP36	J4—36	186	J4—TP74	J4—74	869
J4—TP36	S9C—1	275	J4—TP75	J4—75	870
J4—TP37	J4—37	187	J4—TP76	J4—76	871
J4—TP37	S9C—2	276	J4—TP77	J4—77	872
J4—TP38	J4—38	188	J4—TP78	J4—78	873
J4—TP38	S9C—3	277	J4—TP79	J4—79	874
J4—TP39	J4—39	852	J4—TP80	J4—80	875
J4—TP40	J4—40	853	J4—TP81	J4—81	876
J4—TP41	J4—41	854	J4—TP82	J4—82	877
J4—TP42	J4—42	855	J4—TP83	J4—83	878
J4—TP43	J4—43	856	J4—TP84	J4—84	205
J4—TP44	J4—44	857	J4—TP84	S9C—W3	293
J4—TP45	J4—45	858	J4—TP85	J4—85	879
J4—TP46	E37	436	J4—TP86	J4—86	880
J4—TP46	J4—46	860	J4—TP87	J4—87	881
J4—TP46	XA5—7	562	J4—TP88	J4—88	882
J4—TP47	J4—47	567	J4—TP89	NC	
J4—TP47	VR3 AD	478	J4—TP90	NC	
J4—TP47	XA6—C	598	J4—TP91	NC	
J4—TP48	J4—48	515	J4—TP92	NC	
J4—TP48	XA5—15	424	J4—TP93	J4—93	206
J4—TP49	J4—49	189	J4—TP93	S9C—2	294
J4—TP49	XA7—7	278	J4—TP94	NC	
J4—TP50	J4—50	190	J4—TP95	J4—95	207
J4—TP50	XA7—8	279	J4—TP95	S9A—W3	295
J4—TP51	J4—51	859	J4—TP96	J4—96	208
J4—TP52	J4—52	191	J4—TP96	S9A—W4	296
J4—TP52	R31—8	280	J4—TP97	J4—97	209
J4—TP53	J4—53	192	J4—TP97	XA1—8	297
J4—TP53	S9C—W4	281	J4—TP98	NC	
J4—TP54	J4—54	193	J4—TP99	NC	
J4—TP54	XA1—X	378	J4—TP100	NC	
J4—TP55	J4—55	194	J4—TP101	E7	435
J4—TP55	XA1—Z	312	J4—TP101	J4—101	417
J4—TP56	J4—56	195	J4—1	J4—TP1	482
J4—TP56	S9D—W3	284	J4—2	J4—TP2	414
J4—TP57	J4—57	196	J4—3	J4—TP3	837
J4—TP57	S9D—7	285	J4—4	J4—TP4	838

Table 3-43. Test Set Subassembly MX-8639A/APS-94D, Unit 2 Wire List - Continued

From—	To—	Wire No.	From—	To—	Wire No.
J4—5	J4—TP5	839	J4—66	J4—TP66	865
J4—6	J4—TP6	840	J4—67	J4—TP67	200
J4—7	J4—TP7	841	J4—68	J4—TP68	201
J4—8	J4—TP8	177	J4—69	J4—TP69	202
J4—9	J4—TP9	178	J4—70	J4—TP70	204
J4—10	J4—TP10	179	J4—71	J4—TP71	866
J4—11	J4—TP11	415	J4—72	J4—TP72	867
J4—12	J4—TP12	497	J4—73	J4—TP73	868
J4—13	J4—TP13	585	J4—74	J4—TP74	869
J4—14	J4—TP14	842	J4—75	J4—TP75	870
J4—15	J4—TP15	843	J4—76	J4—TP76	871
J4—16	J4—TP16	844	J4—77	J4—TP77	872
J4—17	J4—TP17	180	J4—78	J4—TP78	873
J4—18	J4—TP18	181	J4—79	J4—TP79	874
J4—19	J4—TP19	845	J4—80	J4—TP80	875
J4—20	J4—TP20	498	J4—81	J4—TP81	876
J4—21	J4—TP21	499	J4—82	J4—TP82	877
J4—22	J4—TP22	846	J4—83	J4—TP83	878
J4—23	J4—TP23	416	J4—84	J4—TP84	205
J4—24	J4—TP24	182	J4—85	J4—TP85	879
J4—25	J4—TP25	183	J4—86	J4—TP86	880
J4—26	J4—TP26	549	J4—87	J4—TP87	881
J4—27	J4—TP27	847	J4—88	J4—TP88	881
J4—28	J4—TP28	848	J4—89	NC	
J4—29	J4—TP29	13	J4—90	NC	
J4—30	J4—TP30	586	J4—91	NC	
J4—31	J4—TP31	849	J4—92	NC	
J4—32	J4—TP32	850	J4—93	J4—TP93	206
J4—33	J4—TP33	851	J4—94	NC	
J4—34	J4—TP34	184	J4—95	J4—TP95	207
J4—35	J4—TP35	185	J4—96	J4—TP96	208
J4—36	J4—TP36	186	J4—97	J4—TP97	209
J4—37	J4—TP37	187	J4—98	NC	
J4—38	J4—TP38	188	J4—99	NC	
J4—39	J4—TP39	852	J4—100	NC	
J4—40	J4—TP40	853	J4—101	J4—TP101	417
J4—41	J4—TP41	854	J5—TP1	E12	639
J4—42	J4—TP42	855	J5—TP1	J5—1	630
J4—43	J4—TP43	856	J5—TP2	E13	640
J4—44	J4—TP44	857	J5—TP2	J5—2	631
J4—45	J4—TP45	858	J5—TP3	E14	641
J4—46	J4—TP46	550	J5—TP3	J5—3	332
J4—47	J4—TP47	587	J5—TP4	NC	
J4—48	J4—TP48	515	J5—TP5	NC	
J4—49	J4—TP49	189	J5—TP6	C4 NEG	539
J4—50	J4—TP50	190	J5—TP6	J5—6	568
J4—51	J4—TP51	859	J5—TP7	NC	
J4—52	J4—TP52	191	J5—TP8	C1 POS	563
J4—53	J4—TP53	192	J5—TP8	J5—8	575
J4—54	J4—TP54	193	J5—TP9	NC	
J4—55	J4—TP55	194	J5—TP10	E25	600
J4—56	J4—TP56	195	J5—TP10	J5—10	589
J4—57	J4—TP57	196	J5—TP11	J1—TP39	562
J4—58	J4—TP58	197	J5—TP11	J5—11	561
J4—59	J4—TP59	198	J5—TP12	J1—TP40	563
J4—60	J4—TP60	199	J5—TP12	J5—12	454
J4—61	J4—TP61	860	J5—TP13	J1—TP21	458
J4—62	J4—TP62	861	J5—TP13	J5—13	455
J4—63	J4—TP63	862	J5—TP14	E16	523
J4—64	J4—TP64	863	J5—TP14	J5—14	516
J4—65	J4—TP65	864	J5—TP15	J5—15	15

Table 3-43. Test Set Subassembly MX-8639A/APS-94D, Unit 2 Wire List - Continued

From—	To—	Wire No.	From—	To—	Wire No.
J5—TP16	J5—16	16	R5—B	S4—4	366
J5—TP17	NC		R5—C	R5—B	775
J5—TP18	J1—TP22	459	R6—A	XA6—W	610
J5—TP18	J5—18	456	R6—B	E3	428
J5—TP19	NC		R6—C	S3—W5	368
J5—TP20	NC		R8—A	XA1—2	379
J5—TP21	NC		R8—B	E2	792
J5—TP22	NC		R8—B	XA1—T	308
J5—TP23	NC		R9—1	TB3—3	351
J5—TP24	NC		R9—2	S9C—10	370
J5—TP25	NC		R9—3	TB3—4	352
J5—TP26	NC		R10—1	TB3—1	353
J5—1	J5—TP1	630	R10—2	R21—1	350
J5—2	J5—TP2	631	R10—3	TB3—12	354
J5—3	J5—TP3	632	R11—1	TB3—14	356
J5—4	NC		R11—2	XA1—L	302
J5—5	NC		R11—3	TB3—13	355
J5—6	J5—TP6	588	R12—1	TB3—16	358
J5—7	NC		R12—2	S9C—12	371
J5—8	J5—TP8	575	R12—3	TB3—15	357
J5—9	NC		R21—1	R10—2	350
J5—10	J5—TP10	589	R21—1	R21—2	764
J5—11	J5—TP11	551	R21—2	R21—1	764
J5—12	J5—TP12	454	R21—3	J4—TP52	280
J5—13	J5—TP13	455	S2—3	R2—C	
J5—14	J5—TP14	516	S2—2	XA2—A	326
J5—15	J5—TP15	15	S2—1	XA2—E	
J5—16	J5—TP16	16	S2—4	R3—B	363
J5—17	NC		S2—4	TP1	364
J5—18	J5—TP18	456	S2—5	XA2—F	327
J5—19	NC		S2—6	XA2—C	331
J5—20	NC		S3—W1	XA2—U	680A
J5—21	NC		S3—W2	XA2—V	680B
J5—22	NC		S3—W3	XA3—U	681A
J5—23	NC		S3—W4	XA3—V	681B
J5—24	NC		S3—W5	R6—C	368
J5—25	NC		S3—W6	NC	
J5—26	NC		S3—1	J1—TP1	670A
Q1—B	XA6—20	570	S3—2	J1—TP5	671B
Q1—C	TB3—11	462	S3—3	J1—TP2	670B
Q1—C	XA6—V	461	S3—4	J1—TP4	671A
Q1—E	S8C—W1	319	S3—5	J1—TP7	672A
Q1—E	XA6—D	430	S3—6	J1—TP11	673B
Q1—E	XA7—12	467	S3—7	J1—TP8	672B
Q2—B	XA6—21	611	S3—8	J1—TP10	673A
Q2—C	TB3—10	477	S3—9	XA1—X	282
Q2—C	XA6—X	476	S3—10	XA1—Z	283
Q2—E	XA6—E	475	S3—11	NC	
R2—A	XA1—S	307	S3—12	NC	
R2—B	XA1—16	320	S4—1	R4—C	365
R2—C	S2—3	362	S4—2	XA3—A	328
R3—B	R3—C	774	S4—3	XA3—E	329
R3—A	TB3—26	387	S4—4	R5—B	366
R3—A	XA2—B	658	S4—4	TP2	367
R3—B	S2—4	363	S4—5	XA3—F	330
R3—C	R3—B	774	S4—6	XA3—C	380
R4—A	XA1—R	306	S5—2	J4—TP21	506
R4—B	XA1—13	317	S5—1	NC	
R4—C	S4—1	365	S5—3	J4—TP20	505
R5—B	R5—C	775	S5—3	XDS4—1	369
R5—A	XA3—B	668	S6—1	NC	

Table 3-43. Test Set Subassembly MX-8639A/APS-94D, Unit 2 Wire List - Continued

From—	To—	Wire No.	From	To—	Wire No.
S6-2	S6-5	777	S8B-6	S8B-8	821
S6-2	XA7-12	571	S8B-7	S8B-5	822
S6-3	XA5-8	333	S8B-7	XA1-7	312
S6-4	S6-6	778	S8B-8	S8B-6	821
S6-5	S6-2	777	S8B-8	S8B-9	826
S6-6	S6-4	778	S8B-9	S8B-8	826
S6-6	XA5-10	334	S8B-9	XA1-F	298
S7-W1	J1-TP61	388	S8B-10	S9B-W2	781
S7-W2	B2-2	376	S8B-11	S9B-W1	780
S7-W3	S12-2	373	S8B-12	S9A-W1	779
S7-W4	B2-4	374	S8C-W1	Q1-E	319
S7-W5	B2-3	375	S8C-W1	S9C-W1	794
S7-W6	B2-1	372	S8C-1	J4-TP36	275
S7-1	E38	380	S8C-2	J4-TP37	276
S7-2	E7	705	S8C-3	J4-TP38	277
S7-3	XA5-N	701B	S9A-W1	S8B-12	779
S7-4	XA5-D	700B	S9A-W2	J4-TP68	290
S7-5	XA5-M	701A	S9A-W3	J4-TP65	295
S7-6	XA5-E	700C	S9A-W4	J4-TP66	296
S7-7	XA5-P	701C	S9A-1	S9A-3	798
S7-8	XA5-C	700A	S9A-2	XA7-13	339
S7-9	XA5-R	683A	S9A-3	S9A-1	798
S7-10	XA5-B	682B	S9A-3	S9B-2	799
S7-11	XA5-S	683B	S9A-4	S8B-W2	789
S7-12	XA5-A	682A	S9A-4	S9A-6	813
S8A-W1	S9A-8	786	S9A-5	S8B-W3	790
S8A-W2	S9A-10	788	S9A-6	S9A-4	813
S8A-W3	S9A-11	787	S9A-7	S9A-9	811
S8A-W4	S9A-9	785	S9A-8	S8A-W1	786
S8A-1	S8A-6	824	S9A-9	S8A-W4	785
S8A-1	S8A-11	825	S9A-9	S9A-7	811
S8A-2	S8A-3	814	S9A-10	S8A-W2	788
S8A-2	S8A-10	815	S9A-10	S9A-12	812
S8A-3	S8A-2	814	S9A-11	S8A-W3	787
S8A-3	S8A-4	817	S9A-12	S9A-10	812
S8A-4	S8A-3	817	S9B-W1	S8B-11	780
S8A-4	S8A-5	818	S9B-W2	S8B-10	781
S8A-5	S8A-4	818	S9B-W3	S8B-2	783
S8A-5	S8A-7	819	S9B-W4	S8B-3	782
S8A-6	S8A-1	824	S9B-1	S9B-3	800
S8A-6	S8A-8	823	S9B-2	S9A-3	799
S8A-7	S8A-5	819	S9B-2	XA7-22	346
S8A-7	XA1-6	314	S9B-3	S9B-1	800
S8A-8	E1	533	S9B-3	S9B-5	801
S8A-8	S8A-6	823	S9B-4	S9B-6	802
S8A-8	S8A-9	820	S9B-4	XA6-M	337
S8A-9	S8A-8	820	S9B-5	S9B-3	801
S8A-10	S8A-2	815	S9B-5	XA7-14	340
S8A-10	S8A-12	816	S9B-6	S9B-4	802
S8A-11	S8A-1	825	S9B-6	XA7-21	345
S8A-12	S8A-10	816	S9B-7	S9B-9	805
S8A-12	XA6-V	653	S9B-8	S9B-12	804
S8B-W1	XA6-P	664	S9B-8	XA7-20	344
S8B-W2	S9A-4	789	S9B-9	S9B-7	805
S8B-W3	S9A-5	790	S9B-9	S9C-5	806
S8B-W4	XA6-F	662	S9B-10	S9B-12	803
S8B-1	S9C-W2	784	S9B-11	XA7-16	341
S8B-2	S9B-W3	783	S9B-12	S9B-8	804
S8B-3	S9B-W4	782	S9B-12	S9B-10	803
S8B-4	XA1-H	299	S9C-W1	S8C-W1	794
S8B-5	S8B-7	822	S9C-W2	S8B-1	784

Table 3-43. Test Set Subassembly MX-8639A/APS-94D, Unit 2 Wire List - Continued

From—	To—	Wire No.	From—	To—	Wire No.
XA1—14	XA7—F	318	XA4—D	J3—TP59	654
XA1—15	NC		XA4—E	J3—TP58	653
XA1—16	R2—B	320	XA4—F	650 SHLD	738
XA1—17	S11—9	321	XA4—H	654 SHLD	740
XA1—18	XA6—U	324	XA4—H	678 SHLD	741
XA1—19	S11—8	323	XA4—J	XA3—B	659
XA1—20	NC		XA4—K	XA1—B	656
XA1—21	J4—TP13	603	XA4—K	XA2—B	657
XA1—22	NC		XA4—L	E11	606
XA2—A	S2—2	325	XA4—M	E22	661
XA2—B	R3—A	658	XA4—N	J2—TP13	223
XA2—B	XA4—K	657	XA4—P	J3—TP53	678A
XA2—C	S2—6	381	XA4—R	J3—TP52	678B
XA2—D	657 SHLD	728	XA4—S	NC	
XA2—D	658 SHLD	729	XA4—1	E24	607
XA2—E	S2—1	326	XA4—2	E21	567
XA2—F	S2—5	327	XA4—3	NC	
XA2—H	NC		XA4—4	NC	
XA2—J	NC		XA4—5	NC	
XA2—K	NC		XA4—6	E16	527
XA2—L	NC		XA4—7	656 SHLD	745
XA2—M	E8	565	XA4—7	679 SHLD	46
XA2—M	XA2—P	730	XA4—8	NC	
XA2—N	E10	604	XA4—9	NC	
XA2—N	XA2—R	731	XA4—10	NC	
XA2—P	XA2—M	730	XA4—11	NC	
XA1—R	XA2—N	731	XA4—12	E9	568
XA2—S	680 SHLD	732	XA4—13	J3—TP64	655
XA2—T	E17	525	XA4—14	J3—TP57	679B
XA2—U	S3—W1	680A	XA4—15	J3—TP56	679A
XA2—V	S3—W2	680B	XA5—A	S7—12	682A
XA2—W	NC		XA5—B	S7—10	682B
XA2—X	NC		XA5—C	S7—8	700A
XA3—A	S4—2	328	XA5—D	S7—4	700B
XA3—B	R5—A	666	XA5—E	S7—6	700C
XA3—B	XA4—J	659	XA5—F	NC	
XA3—C	S4—6	380	XA5—H	XA6—7	752
XA3—D	658 SHLD	734	XA5—H	XA6—2	569
XA3—D	659 SHLD	733	XA5—J	XA7—6	331
XA3—D	666 SHLD	742	XA5—K	J4—TP23	423
XA3—E	S4—3	329	XA5—K	XDS4—2	429
XA3—F	S4—5	330	XA5—L	S9D—8	608
XA3—H	NC		XA5—L	XA6—C	609
XA3—J	NC		XA5—M	S7—5	701A
XA3—K	NC		XA5—N	S7—3	701B
XA3—L	NC		XA5—P	S7—7	701C
XA3—M	E9	566	XA5—R	S7—9	683A
XA3—M	XA3—P	735	XA5—S	S7—11	683B
XA3—N	E11	606	XA5—1	E5	528
XA3—N	XA3—R	736	XA5—2	NC	
XA3—P	XA3—M	735	XA5—3	J4—TP15	332
XA3—R	XA3—N	736	XA5—4	NC	
XA3—S	681 SHLD	737	XA5—5	B1—R1	664A
XA3—T	E17	526	XA5—5	J4—TP1	486
XA3—U	S3—W3	681A	XA5—6	NC	
XA3—V	S3—W4	681B	XA5—7	J4—TP46	562
XA3—W	NC		XA5—7	XA6—H	752
XA3—X	NC		XA5—8	S6—3	333
XA4—A	E20	660	XA5—9	J4—TP12	504
XA4—B	NC		XA5—10	S6—5	334
XA4—C	J1—TP23	650	XA5—11	J4—TP18	335

Table 3-43. Test Set Subassembly MX-8639A/APS-94D, Unit 2 Wire List - Continued

From—	To—	Wire No.	From—	To—	Wire No.
S9C—W3	J4—TP84	280	TB3—12	R10—3	354
S9C—W4	J4—TP83	281	TB3—13	R11—3	355
S9C—1	J4—TP34	273	TB3—14	R11—1	356
S9C—2	J4—TP33	294	TB3—15	R12—3	357
S9C—3	J4—TP35	274	TB3—16	R12—:	358
S9C—4	S9C—5	306	TB3—26	R3—A	287
S9C—4	XA6—J	683	TP1	S2—4	284
S9C—5	S9B—9	306	TP2	S4—4	287
S9C—5	S9C—8	307	VR1 AD	VR2 AD	795
S9C—6	S9C—4	308	VR 1C	XDS1—1	427
S9C—6	S9C—9	309	VR2 AD	VR1 AD	795
S9C—7	S9C—9	310	VR2 AD	VR3 AD	797
S9C—8	S9C—5	307	VR2 C	XDS2—1	430
S9C—8	XA7—17	342	VR3 AD	J4—TP47	475
S9C—9	S9C—6	309	VR3 AD	VR2 AD	[illegible]7
S9C—9	S9C—7	310	VR3 C	XDS3—1	466
S9C—9	XA7—19	343	XA1—A	E17	534
S9C—10	R9—2	370	XA1—A	XA1—1	725
S9C—11	E1	584	XA1—A	666 SHLD	737
S9C—12	R12—2	371	XA1—B	XA4—K	656
S9D—W1	NC		XA1—C	E37	296
S9D—W2	NC		XA1—D	E10	601
S9D—W3	J4—TP56	284	XA1—E	E8	564
S9D—W4	NC		XA1—F	S9B—9	298
S9D—1	NC		XA1—H	S9B—4	299
S9D—2	NC		XA1—J	TB3—2	300
S9D—3	NC		XA1—K	XA6—T	301
S9D—4	NC		XA1—L	R11—2	302
S9D—5	NC		XA1—M	XDS1—2	303
S9D—6	NC		XA1—N	XDS2—2	304
S9D—7	J4—TP57	285	XA1—P	XDS3—2	305
S9D—7	S9D—9		XA1—R	R4—A	306
S9D—8	XA5—L	608	XA1—S	R2—A	307
S9D—9	S9D—7		XA1—T	R3—B	308
S9D—10	NC		XA1—U	S11—8	309
S9D—11	NC		XA1—V	S11—1	383
S9D—12	NC		XA1—V	XA6—S	310
S10—2	E31	463	XA1—W	S11—2	311
S10—3	E37	573	XA1—X	J4—TP54	378
S11—W1	XA6—N	338	XA1—X	S3—9	282
S11—W2	NC		XA1—Y	NC	
S11—W3	XA6—K	336	XA1—Z	J4—TP55	312
S11—1	XA1—V	383	XA1—Z	S3—10	282
S11—2	XA1—W	311	XA1—1	XA1—A	725
S11—3	XA1—19	323	XA1—1	669 SHLD	827
S11—4	NC		XA1—2	R5—A	379
S11—5	NC		XA1—3	NC	
S11—6	NC		XA1—4	NC	
S11—7	E4	430	XA1—5	NC	
S11—8	XA1—U	309	XA1—6	E23	669
S11—9	XA1—17	321	XA1—7	S8B—7	313
S12—2	S7—W3	373	XA1—8	E21	578
S12—3	B2—5	377	XA1—8	J4—TP97	297
TB3—1	R10—1	353	XA1—8	S8A—7	314
TB3—2	XA1—J	300	XA1—9	E34	613
TB3—3	R9—1	351	XA1—9	XA6—X	602
TB3—4	R9—3	352	XA1—10	J4—TP24	271
TB3—5	E4	426	XA1—11	XA7—H	315
TB3—10	Q3—C	477	XA1—12	XA7—J	316
TB3—11	Q1—C	462	XA1—13	R4—B	317

Table 3-43. Test Set Subassembly MX-8639A/APS-94D, Unit 2 Wire List - Continued

From—	To—	Wire No.	From—	To—	Wire No.
XA5-12	J4-TP14	302	XA7-A	E6	531
XA5-13	B1-R2	664B	XA7-A	XA7-1	759
XA5-13	J4-TP2	422	XA7-B	NC	
XA5-14	J4-TP17	269	XA7-C	NC	
XA5-15	J4-TP46	424	XA7-D	NC	
XA6-A	E6	530	XA7-E	NC	
XA6-A	XA6-1	753	XA7-F	XA1-14	318
XA6-A	664 SHLD	758	XA7-H	XA1-11	315
XA6-B	XA5-H	560	XA7-J	XA1-12	316
XA6-B	XA6-D	754	XA7-K	NC	
XA6-C	J4-TP47	598	XA7-L	NC	
XA6-C	XA5-L	609	XA7-M	NC	
XA6-C	XA6-E	755	XA7-N	NC	
XA6-D	Q1-E	460	XA7-P	NC	
XA6-D	XA6-B	754	XA7-R	NC	
XA6-E	Q2-E	475	XA7-S	NC	
XA6-E	XA6-C	755	XA7-T	NC	
XA6-F	S9B-W4	662	XA7-U	NC	
XA6-H	J4-TP59	287	XA7-V	NC	
XA6-J	S9C-4	663	XA7-W	NC	
XA6-K	S11-W3	336	XA7-X	NC	
XA6-L	NC		XA7-Y	NC	
XA6-M	S9B-4	337	XA7-Z	NC	
XA6-N	S11-W1	338	XA7-1	XA7-A	759
XA6-P	S9B-W1	664	XA7-2	J4-TP70	292
XA6-R	J4-TP58	286	XA7-3	J4-TP60	836
XA6-S	XA1-V	310	XA7-4	J4-TP67	289
XA6-T	XA1-K	301	XA7-5	J4-TP25	272
XA6-U	XA1-18	324	XA7-6	XA5-J	331
XA6-V	J4-TP26	561	XA7-7	J4-TP49	278
XA6-V	Q1-C	461	XA7-8	J4-TP50	279
XA6-V	S9A-12	583	XA7-9	J1-TP30	291
XA6-W	J4-TP13	596	XA7-10	NC	
XA6-W	R6-A	610	XA7-11	NC	
XA6-X	J4-TP30	597	XA7-12	Q1-E	467
XA6-X	Q2-C	476	XA7-12	S6-2	571
XA6-X	XA1-9	602	XA7-13	S9A-2	339
XA6-Y	NC		XA7-14	S9B-5	340
XA6-Z	NC		XA7-15	NC	
XA6-1	XA6-A	753	XA7-16	S9B-11	341
XA6-2	NC		XA7-17	S9C-8	342
XA6-3	NC		XA7-18	NC	
XA6-4	NC		XA7-19	S9C-9	343
XA6-5	NC		XA7-20	S9B-8	344
XA6-6	NC		XA7-21	S9B-6	345
XA6-7	NC		XA7-22	S9B-2	346
XA6-8	NC		XDS1-2	E28	359
XA6-9	NC		XDS1-1	VR1-C	427
XA6-10	NC		XDS1-2	XA1-M	303
XA6-11	NC		XDS2-2	E29	360
XA6-12	NC		XDS2-1	VR2-C	428
XA6-13	NC		XDS2-2	XA1-N	304
XA6-14	NC		XDS3-2	E32	361
XA6-15	NC		XDS3-1	VR3-C	406
XA6-16	NC		XDS3-2	XA1-P	305
XA6-17	NC		XDS4-A	S5-3	368
XA6-18	NC		XDS4-B	XA5-K	429
XA6-19	NC		650 SHLD	J1-TP24	706
XA6-20	Q1-B	570	650 SHLD	XA4-F	738
XA6-21	Q2-B	511	651 SHLD	J1-TP38	708
XA6-22	NC		652 SHLD	E18	717

Table 3-43. Test Set Subassembly MX-8639A/APS-94D, Unit 2 Wire List - Continued

From—	To—	Wire No.	From—	To—	Wire No.
652 SHLD	J2—TP47	716	671 SHLD	J1—TP6	703
653 SHLD	654 SHLD	739	672 SHLD	J1—TP9	704
654 SHLD	XA4—H	740	673 SHLD	J1—TP12	706
654 SHLD	653 SHLD	739	674 SHLD	J1—TP24	707
655 SHLD	XA4—7	745	675 SHLD	J2—TP16	712
656 SHLD	XA1—A	727	675 SHLD	J3—TP16	830
657 SHLD	XA2—D	728	676 SHLD	J2—TP19	713
658 SHLD	XA2—D	729	676 SHLD	J3—TP19	831
658 SHLD	XA2—D	731	677 SHLD	J2—TP26	714
659 SHLD	XA3—D	733	678 SHLD	XA4—H	741
660 SHLD	E33	744	679 SHLD	XA4—7	746
661 SHLD	E33	742	680 SHLD	XA2—S	732
662 SHLD	663 SHLD	756	681 SHLD	XA3—S	737
663 SHLD	662 SHLD	756	684 SHLD	E5	749
663 SHLD	664 SHLD	757	695 SHLD	J2—TP7	
664 SHLD	XA6—A	758	695 SHLD	J3—TP7	828
664 SHLD	663 SHLD	757	696 SHLD	J2—TP11	711
666 SHLD	XA3—D	743	696 SHLD	J3—TP11	829
667 SHLD	E33	709	697 SHLD	J2—TP30	715
668 SHLD	E18	719	698 SHLD	J2—TP88	720
668 SHLD	J2—TP50	718	698 SHLD	J3—TP88	
669 SHLD	E33	832	699 SHLD	J4—TP11	725
669 SHLD	XA1—1	827	701 SHLD	E5	751
670 SHLD	J1—TP3	702			

APPENDIX A

REFERENCES

The following applicable publications should be available to direct support personnel for use with Test Set Group, Indicator, Radar OQ-63A/APS-94D.

DA Pam 310-4	Index of Technical Publications: Technical Manuals, Technical Bulletins, Supply Manuals, (Types 7, 8, and 9), Supply Bulletins, and Lubrication Orders.
DA Pam 310-7	US Army Equipment Index of Modification Work Orders.
TB 11-1833-35-1	Calibration Procedure for Radar Indicator Test Set Group OQ-63A/APS-94D (NSN 6625-01-058-7874).
TB 43-0119	Field Instructions for Painting and Preserving Electronics Command Equipment Including Camouflage Pattern Painting of Electrical Equipment Shelters.
TM 11-5895-967-12	Operator's and Organizational Maintenance Manual Radar Surveillance Set AN/APS-94E.
TM 11-6625-444-14-1	Operator's, Organizational, Direct Support and General Support Maintenance Manual Including Repair Parts and Special Tools List: Voltmeter, Digital AN/GSM-64B (NSN 6625-00-022-7894) Including Plug-In, Electronic Test Equipment PL-1370/GSM-64B (NSN 6625-00-137-8366).
TM 11-6625-654-14	Operator's, Organizational, Direct Support, and General Support Maintenance Manual Repair Parts and Special Tools Lists (Including Depot Maintenance Repair Part and Special Tools) for Multimeter AN/USM-223.
TM 11-6625-1833-12	Operator and Organizational Maintenance Manual, Test Set Group, Indicator, Radar OQ-63A/APS-94D.
TM 11-6625-2658-14	Operator's, Organizational, Direct Support and General Support Maintenance Manual for Oscilloscope AN/USM-281C (NSN 6625-00-106-9622).
TM 38-750	The Army Maintenance Management System (TAMMS).

APPENDIX B

EXPENDABLE SUPPLIES AND MATERIALS LIST

Section I. INTRODUCTION

B-1. Scope

This appendix lists expendable supplies and materials you will need to operate and maintain the OQ-63A/APS-94D. These items are authorized to you by CTA 50-970, Expendable Items (Except Medical, Class V, Repair Parts, and Heraldic Items).

B-2. Explanation of Columns

a. Column 1—Item Number. This number is assigned to the entry in the listing and is referenced in the narrative instructions to identify the material (e.g., "Use cleaning compound, item 5, App. D").

b. Column 2—Level. This column identifies the lowest level of maintenance that requires the listed item.

C—Operator/Crew
O—Organizational Maintenance
F—Direct Support Maintenance
H—General Support Maintenance

c. Column 3—National Stock Number. This is the National stock number assigned to the item; use it to request or requisition the item.

d. Column 4—Description. Indicates the Federal item name and, if required, a description to identify the item. The last line for each item indicates the part number followed by the Federal Supply Code for Manufacturer (FSCM) in parentheses, if applicable.

e. Column 5—Unit of Measure (U/M). Indicates the measure used in performing the actual maintenance function. This measure is expressed by a two-character alphabetical abbreviation (e.g., ea, in, pr). If the unit of measure differs from the unit of issue, requisition the lowest unit of issue that will satisfy your requirements.

(Next printed page B-3)

SECTION II EXPENDABLE SUPPLIES AND MATERIALS LIST

(1) ITEM NO.	(2) LEVEL	(3) NATIONAL STOCK NUMBER	(4) DESCRIPTION PART NO AND FSCM	(5) UNIT OF MEAS
1	O	5350-00-264-3485	PAPER, ABRASIVE, FLINT (SANDPAPER, FINE) MIL-PP-105	PKG
2	O	7570-00-933-7372	TAPE, ELECTRICAL (BLACK PLASTIC) 1/2 INCH	ROLL
3	C,O	8020-00-178-8305	BRUSH, PAINT MIL-H-B-420 (81348)	EA
4	O	5350-00-145-0747	PRIMER, COLOR Y PER MIL-P-8585 (81348)	QT
5	O	8010-00-575-0808	ENAMEL, LIGHT GRAY (CLASS-2 - METAL)	GAL
6	C,O	6810-00-551-1487	TRICHLOROETHANE, TECHNICAL, CLEANING COMPOUND O-T-620, TYPE I (81348)	QT
7	C,O	8305-00-285-3436	CLOTH, COTTON, (LINT-FREE) CCC-C-440 (81348)	YD
8	C,O	7920-00-205-2404	BRUSH, CLEANING MIL-B-288 (81348)	EA

INDEX

Paragraph, Figure
Table, Number

	Paragraph, Figure Table, Number

	Paragraph, Figure Table, Number
Negative Sweep Detector 2A4A1AR5 and Unipolarizer A1AR7	2-64, FO-24
Negative Sweep Detector 2A4A2AR2 and Unipolarizer A2AR4	2-68, FO-24
Offset Circuit:	
Bench test	3-27a, T3-24
Troubleshooting	3-27b, T3-25
Organization of Direct Support Maintenance	3-2
Organization of Troubleshooting Procedures	3-5
Oscillator, Five-MHz	2-51, FO-15
Overvoltage Protection Circuit	2-11, 2-40 F2-2, F2-6
Painting	3-39
Physical Tests and Inspections	3-45
Programable Read Only Memory (PROM) and Data Selection	2-93g
Publications, Index	1-2
Radar Indicating System CRT Sweep Requirements	2-3, F2-1
Ramp Generator Circuit	2-93l
Records, Forms	1-3
Regulated +28 Volt DC Supply and High Voltage Loads	2-91, F2-9
Regulated Plus and Minus 9-Volt Source	2-27, FO-2
Removal and Replacement Procedure:	
MX-8638A/APS-94D Unit 1A1	3-36a
MX-8638A/APS-94D Unit 1A2	3-36b
MX-8639A/APS-94D Unit 2	3-36c
Repair Procedures	3-36
Reporting Equipment Improvement Recommendations (EIR)	1-4
Report of Packaging and Handling Deficiency	1-3b
Reports of Maintenance and Unsatisfactory Equipment	1-3a
Reset Circuit	2-93c
Reset Pulse Generation	2-54, FO-15
Secondary Power Sources	2-87, FO-8, FO-26
Scope	1-1
Scope of Direct Support Maintenance	3-1
Selectable Compressor Networks	T2-1
Servo Amplifier	2-80, FO-25
Servocontrol Synchro Coarse Calibration	3-41
Servocontrol Synchro Fine Calibration	3-42
SERVO FAULT Light Indications	3-10
Servo Loop:	
Bench test	3-19c, T3-9
Circuit analysis	2-80, FO-3, FO-25
Supplementary test	3-20, T3-11
Troubleshooting	3-19B, T3-10
Servo Loop Stepper Motor	2-81, F2-17
Servo Loop Supplementary Tests	3-20, T3-11
Servo Synchro Coarse Calibration	3-41
Servo Synchro Fine Calibration	3-42
750-Hz Prf Clocked Counter	2-52, FO-15
750-Hz Prf Generation	2-53, 2-12, FO-15
Signal Generation, A Sine θ/A Cosine θ	2-18, FO-2
Signal Generation, Circuit Analysis:	
Reset pulse	2-54

Paragraph, Figure
Table, Number

RECOMMENDED CHANGES TO EQUIPMENT TECHNICAL MANUALS

SOMETHING WRONG WITH THIS MANUAL?

THEN. . .JOT DOWN THE DOPE ABOUT IT ON THIS FORM, TEAR IT OUT, FOLD IT AND DROP IT IN THE MAIL!

FROM: (YOUR UNIT'S COMPLETE ADDRESS)
Commander
Stateside Army Depot
ATTN: AMSTA-US
Stateside, N.J. 07703

DATE 10 July 1975

PUBLICATION NUMBER	DATE	TITLE
TM 11-5840-340-12	23 Jan 74	Radar Set AN/[illegible]-76

BE EXACT. . .PIN-POINT WHERE IT IS				IN THIS SPACE TELL WHAT IS WRONG AND WHAT SHOULD BE DONE ABOUT IT:
PAGE NO.	PARAGRAPH	FIGURE NO.	TABLE NO.	
2-25	2-28			Recommend that the installation antenna alignment procedure be changed throughout to specify a 2° IFF antenna lag rather than 1°. REASON: Experience has shown that with only a 1° lag, the antenna servo system is too sensitive to wind gusting in excess of [illegible] knots, and has a tendency to rapidly accelerate and decelerate as it hunts, causing strain to the drive train. Hunting is minimized by adjusting the lag to 2° without degradation of operation.
3-10	3-3		3-1	Item 5, Function column. Change "2 db" to "3db " REASON: The adjustment procedure for the TRANS POWER FAULT indicator calls for a 3 db (500 watts) adjustment to light the TRANS POWER FAULT indicator.
5-6	5-8			Add new step f.1 to read, "Replace cover plate removed in step e.1, above." REASON: To replace the cover plate.
		FO3		Zone C 3. On J1-2, change "+24 VDC to "+5 VDC." REASON: This is the output line of the 5 VDC power supply. + 24 VDC is the input voltage.

TYPED NAME, GRADE OR TITLE, AND TELEPHONE NUMBER	SIGN HERE:
SSG I. M. DeSpiritof 999-1776	SSG. I.M. DeSpiritof.

DA FORM 1 AUG 74 2028-2

P.S.--IF YOUR OUTFIT WANTS TO KNOW ABOUT YOUR MANUAL "FINDS," MAKE A CARBON COPY OF THIS AND GIVE IT TO YOUR HEADQUARTERS.

TEAR ALONG DOTTED LINE

RECOMMENDED CHANGES TO EQUIPMENT TECHNICAL MANUALS

SOMETHING WRONG WITH THIS MANUAL?

FROM: (YOUR UNIT'S COMPLETE ADDRESS)

DATE

PUBLICATION NUMBER	DATE	TITLE
TM 11-6625-1833-30	25 APR 79	Test Set Group, Indicator Radar OQ-63A/APS-94D

BE EXACT. . .PIN-POINT WHERE IT IS				IN THIS SPACE TELL WHAT IS WRONG AND WHAT SHOULD BE DONE ABOUT IT:
PAGE NO.	PARA-GRAPH	FIGURE NO.	TABLE NO.	

TYPED NAME, GRADE OR TITLE, AND TELEPHONE NUMBER	SIGN HERE.

DA FORM 1 AUG 74 2028-2

P.S.--IF YOUR OUTFIT WANTS TO KNOW ABOUT YOUR MANUAL "FIND" MAKE A CARBON COPY OF THIS AND GIVE IT TO YOUR HEADQUARTERS.

TEAR ALONG DOTTED LINE

FILL IN YOUR UNIT'S ADDRESS

FOLD BACK

DEPARTMENT OF THE ARMY

OFFICIAL BUSINESS

PENALTY FOR PRIVATE USE, $300

POSTAGE AND FEES PAID
DEPARTMENT OF THE ARMY
DOD-314

Commander
US Army Communications and
Electronics Material Readiness Command
ATTN: DRSEL-ME-MQ
Fort Monmouth, New Jersey 07703

FOLD BACK

TEAR ALONG DOTTED LINE

REVERSE OF DA FORM 2028-2

RECOMMENDED CHANGES TO EQUIPMENT TECHNICAL MANUALS

SOMETHING WRONG WITH THIS MANUAL?

FROM: (YOUR UNIT'S COMPLETE ADDRESS)

DATE

PUBLICATION NUMBER	DATE	TITLE
TM 11-6625-1833-30	25 APR 79	Test Set Group, Indicator Radar OQ-634/APS-94D

BE EXACT...PIN-POINT WHERE IT IS				IN THIS SPACE TELL WHAT IS WRONG AND WHAT SHOULD BE DONE ABOUT IT:
PAGE NO.	PARA-GRAPH	FIGURE NO.	TABLE NO.	

TYPED NAME, GRADE OR TITLE, AND TELEPHONE NUMBER	SIGN HERE:

DA FORM 1 AUG 74 2028-2

P.S.--IF YOUR OUTFIT WANTS TO KNOW ABOUT YOUR MANUAL "FIND," MAKE A CARBON COPY OF THIS AND GIVE IT TO YOUR HEADQUARTERS.

TEAR ALONG DOTTED LINE

FILL IN YOUR UNIT'S ADDRESS

FOLD BACK

DEPARTMENT OF THE ARMY

OFFICIAL BUSINESS

PENALTY FOR PRIVATE USE, $300

POSTAGE AND FEES PAID
DEPARTMENT OF THE ARMY
DOD-314

Commander
US Army Communications and
Electronics Material Readiness Command
ATTN: DRSEL-ME-MQ
Fort Monmouth, New Jersey 07703

TEAR ALONG DOTTED LINE

FOLD BACK

REVERSE OF DA FORM 2028-2

RECOMMENDED CHANGES TO EQUIPMENT TECHNICAL MANUALS

SOMETHING WRONG WITH THIS MANUAL?

THEN. . .JOT DOWN THE DOPE ABOUT IT ON THIS FORM, TEAR IT OUT, FOLD IT AND DROP IT IN THE MAIL!

FROM: (YOUR UNIT'S COMPLETE ADDRESS)

DATE

PUBLICATION NUMBER	DATE	TITLE
TM 11-6625-1833-30	25 APR 79	Test Set Group, Indicator Radar OQ-63A/APS-94D

BE EXACT. . .PIN-POINT WHERE IT IS

PAGE NO.	PARA-GRAPH	FIGURE NO.	TABLE NO.	IN THIS SPACE TELL WHAT IS WRONG AND WHAT SHOULD BE DONE ABOUT IT:

TYPED NAME, GRADE OR TITLE, AND TELEPHONE NUMBER	SIGN HERE:

TEAR ALONG DOTTED LINE

DA FORM 1 AUG 74 2028-2

P.S.--IF YOUR OUTFIT WANTS TO KNOW ABOUT YOUR MANUAL "FIND," MAKE A CARBON COPY OF THIS AND GIVE IT TO YOUR HEADQUARTERS.

FILL IN YOUR UNIT'S ADDRESS

FOLD BACK

DEPARTMENT OF THE ARMY

OFFICIAL BUSINESS
PENALTY FOR PRIVATE USE, $300

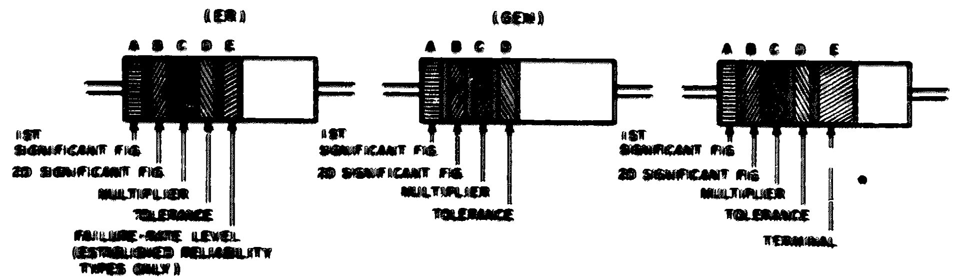
POSTAGE AND FEES PAID
DEPARTMENT OF THE ARMY
DOD-314

Commander
US Army Communications and
Electronics Materiel Readiness Command
ATTN: DRSEL-ME-MQ
Fort Monmouth, New Jersey 07703

TEAR ALONG DOTTED LINE

FOLD BACK

REVERSE OF DA FORM 2028-2



COLOR CODE MARKING FOR COMPOSITION TYPE RESISTORS.

COLOR-CODE MARKING FOR FILM-TYPE RESISTORS

TABLE I
COLOR CODE FOR COMPOSITION TYPE AND FILM TYPE RESISTORS.

BAND A		BAND B		BAND C		BAND D		BAND E		
COLOR	FIRST SIGNIFICANT FIGURE	COLOR	SECOND SIGNIFICANT FIGURE	COLOR	MULTIPLIER	COLOR	RESISTANCE TOLERANCE (PERCENT)	COLOR	FAILURE RATE LEVEL	TERM
BLACK	0	BLACK	0	BLACK	1			BROWN	M=1.0	
BROWN	1	BROWN	1	BROWN	10			RED	P=0.1	
RED	2	RED	2	RED	100			ORANGE	R=0.01	
ORANGE	3	ORANGE	3	ORANGE	1,000			YELLOW	S=0.001	
YELLOW	4	YELLOW	4	YELLOW	10,000	SILVER	±10 (COMP. TYPE ONLY)	WHITE		SOLD-ERABLE
GREEN	5	GREEN	5	GREEN	100,000	GOLD	±5			
BLUE	6	BLUE	6	BLUE	1,000,000	RED	±2 (NOT APPLICABLE TO ESTABLISHED RELIABILITY)			
PURPLE (VIOLET)	7	PURPLE (VIOLET)	7							
GRAY	8	GRAY	8	SILVER	0.01					
WHITE	9	WHITE	9	GOLD	0.1					

BAND A — THE FIRST SIGNIFICANT FIGURE OF THE RESISTANCE VALUE (BANDS A THRU D SHALL BE OF EQUAL WIDTH.)

BAND B — THE SECOND SIGNIFICANT FIGURE OF THE RESISTANCE VALUE

BAND C — THE MULTIPLIER (THE MULTIPLIER IS THE FACTOR BY WHICH THE TWO SIGNIFICANT FIGURES ARE MULTIPLIED TO YIELD THE NOMINAL RESISTANCE VALUE.)

BAND D — THE RESISTANCE TOLERANCE.

BAND E — WHEN USED ON COMPOSITION RESISTORS, BAND E INDICATES ESTABLISHED RELIABILITY FAILURE-RATE LEVEL (PERCENT FAILURE PER 1,000 HOURS). ON FILM RESISTORS, THIS BAND SHALL BE APPROXIMATELY 1-1/2 TIMES THE WIDTH OF OTHER BANDS, AND INDICATES TYPE OF TERMINAL.

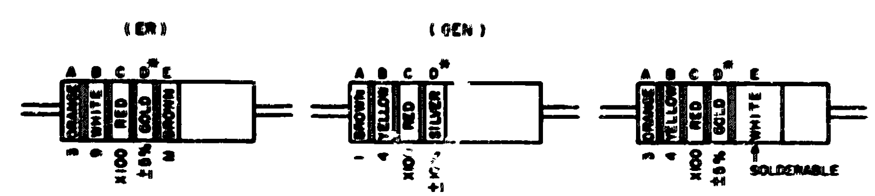
RESISTANCES IDENTIFIED BY NUMBERS AND LETTERS
(THESE ARE NOT COLOR CODED)

SOME RESISTORS ARE IDENTIFIED BY THREE OR FOUR DIGIT ALPHA NUMERIC DESIGNATORS. THE LETTER R IS USED IN PLACE OF A DECIMAL POINT WHEN FRACTIONAL VALUES OF AN OHM ARE EXPRESSED. FOR EXAMPLE

2R7 = 2.7 OHMS   10R0 = 10.0 OHMS

FOR WIRE-WOUND-TYPE RESISTORS COLOR CODING IS NOT USED. IDENTIFICATION MARKING IS SPECIFIED IN EACH OF THE APPLICABLE SPECIFICATIONS

EXAMPLES OF COLOR CODING



NOMINAL RESISTANCE 3,900 OHMS
RESISTANCE TOLERANCE ±5%
FAILURE RATE LEVEL M

NOMINAL RESISTANCE 1,400 OHMS
RESISTANCE TOLERANCE ±10%

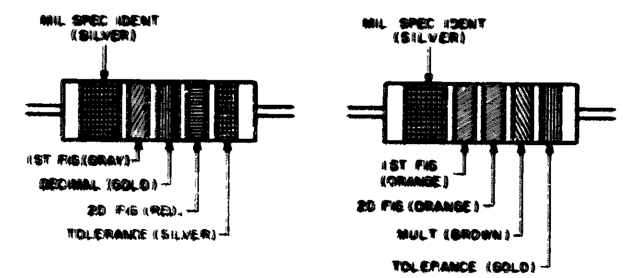
NOMINAL RESISTANCE 3,400 OHMS
RESISTANCE TOLERANCE ±5%
TERMINAL SOLDERABLE

COMPOSITION-TYPE RESISTORS

FILM-TYPE RESISTORS

* IF BAND D IS OMITTED, THE RESISTOR TOLERANCE IS ±20% AND THE RESISTOR IS NOT MIL-STD

A. COLOR CODE MARKING FOR MILITARY STANDARD RESISTORS



(A) 8.2UH ± 10%

(B) 330UH ± 5%

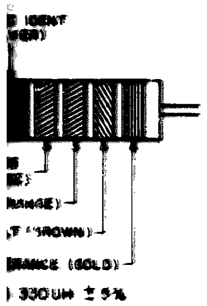
COLOR CODING FOR TUBULAR ENCAPSULATED RF CHOKES. AT A, AN EXAMPLE OF OF THE CODING FOR AN 8.2UH CHOKE IS GIVEN. AT B, THE COLOR BANDS FOR A 330UH INDUCTOR ARE ILLUSTRATED

TABLE 2
COLOR CODING FOR TUBULAR ENCAPSULATED RF CHOKES

COLOR	SIGNIFICANT FIGURE	MULTIPLIER	INDUCTANCE TOLERANCE (PERCENT)
BLACK	0	1	
BROWN	1	10	1
RED	2	100	2
ORANGE	3	1,000	3
YELLOW	4		
GREEN	5		
BLUE	6		
VIOLET	7		
GRAY	8		
WHITE	9		
NONE			20
SILVER			10
GOLD	DECIMAL POINT		5

MULTIPLIER IS THE FACTOR BY WHICH THE TWO COLOR FIGURES ARE MULTIPLIED TO OBTAIN THE INDUCTANCE VALUE OF THE CHOKE COIL

B. COLOR CODE MARKING FOR MILITARY STANDARD INDUCTORS



IES. AT A, AN EXAMPLE OF
F B, THE COLOR BANDS FOR

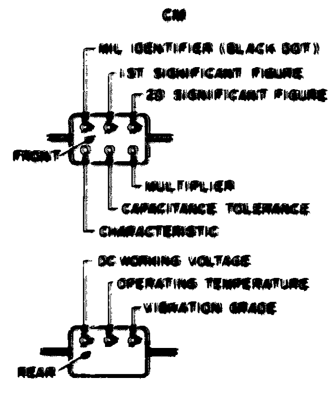
LATED RF CHOKES

INDUCTANCE TOLERANCE (PERCENT)
1
2
3
20
10
5

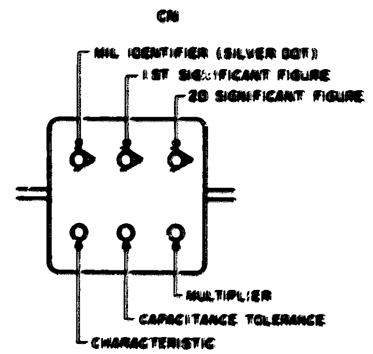
E TWO COLOR FIGURES
CE VALUE OF THE

STANDARD INDUCTORS.

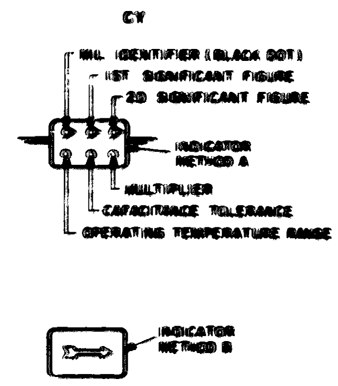
CAPACITORS, FIXED, VARIOUS-DIELECTRICS, STYLES CM, CN, CY, AND CB.



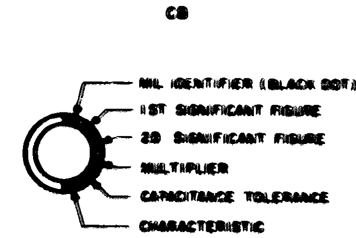
MICA-DIELECTRIC



PAPER-DIELECTRIC



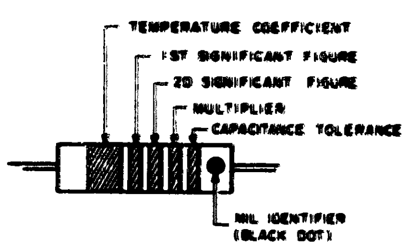
GLASS-DIELECTRIC, GLASS CASE



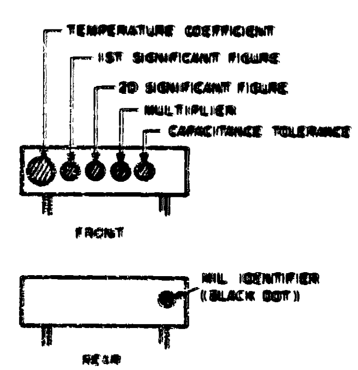
MICA, BUTTON TYPE

TABLE 3 — FOR USE WITH STYLES CM, CN, CY AND CB.

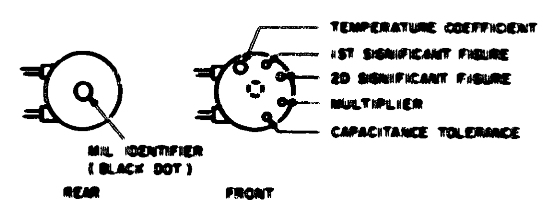
COLOR	MIL ID	1ST SIG FIG	2D SIG FIG	MULTIPLIER[1]	CAPACITANCE TOLERANCE				CHARACTERISTIC[2]			DC WORKING VOLTAGE	OPERATING TEMP RANGE	VIBRATION GRADE
					CM	CN	CY	CB	CM	CN	CB	CM	CY, CM	CM
BLACK	CM CY CB	0	0	1			±20%	±20%		A			-55° TO +70°C	10-55 HZ
BROWN		1	1	10					B	E	B			
RED		2	2	100	±2%		±2%	±2%	C				-55° TO +85°C	
ORANGE		3	3	1,000		±30%			D		D	300		
YELLOW		4	4	10,000					E				-55° TO +125°C	10 2,000 HZ
GREEN		5	5		±5%				F			500		
BLUE		6	6										-55° TO +150°C	
PURPLE (VIOLET)		7	7											
GRAY		8	8											
WHITE		9	9											
GOLD				0.1			±5%	±5%						
SILVER	CN			0.01	±10%	±10%	±10%	±10%						



AXIAL LEAD



RADIAL LEAD



DISK-TYPE

TABLE 4 — TEMPERATURE COMPENSATING, STYLE CC

COLOR	TEMPERATURE COEFFICIENT[4]	1ST SIG FIG	2D SIG FIG	MULTIPLIER[1]	CAPACITANCE TOLERANCE		MIL ID
					CAPACITANCES OVER 10 UUF	CAPACITANCES 10 UUF OR LESS	
BLACK	0	0	0	1		±2.0 UUF	CC
BROWN	−30	1	1	10	±1%		
RED	−80	2	2	100	±2%	±0.25 UUF	
ORANGE	−150	3	3	1,000			
YELLOW	−220	4	4				
GREEN	−330	5	5		±5%	±0.5 UUF	
BLUE	−470	6	6				
PURPLE (VIOLET)	−750	7	7				
GRAY		8	8	0.01*			
WHITE		9	9	0.1*	±10%		
GOLD	+100			0.1		±1.0 UUF	
SILVER				0.01			

1 THE MULTIPLIER IS THE NUMBER BY WHICH THE TWO SIGNIFICANT (SIG) FIGURES ARE MULTIPLIED TO OBTAIN THE CAPACITANCE IN UUF

2 LETTERS INDICATE THE CHARACTERISTICS DESIGNATED IN APPLICABLE SPECIFICATIONS MIL-C-5, MIL-C-25D, MIL-C-11272B, AND MIL-C-10950C RESPECTIVELY

3 LETTERS INDICATE THE TEMPERATURE RANGE AND VOLTAGE-TEMPERATURE LIMITS DESIGNATED IN MIL-C-11015D

4 TEMPERATURE COEFFICIENT IN PARTS PER MILLION PER DEGREE CENTIGRADE

* OPTIONAL CODING WHERE METALLIC PIGMENTS ARE UNDESIRABLE

C. COLOR CODE MARKING FOR MILITARY STANDARD CAPACITORS

ESC-FM 913 73

Figure FO-1. Color Code markings for inductors, resistors, and capacitors

PANEL MARKING FOR EACH CONNECTOR IS LISTED BELOW.

UNIT 1A1

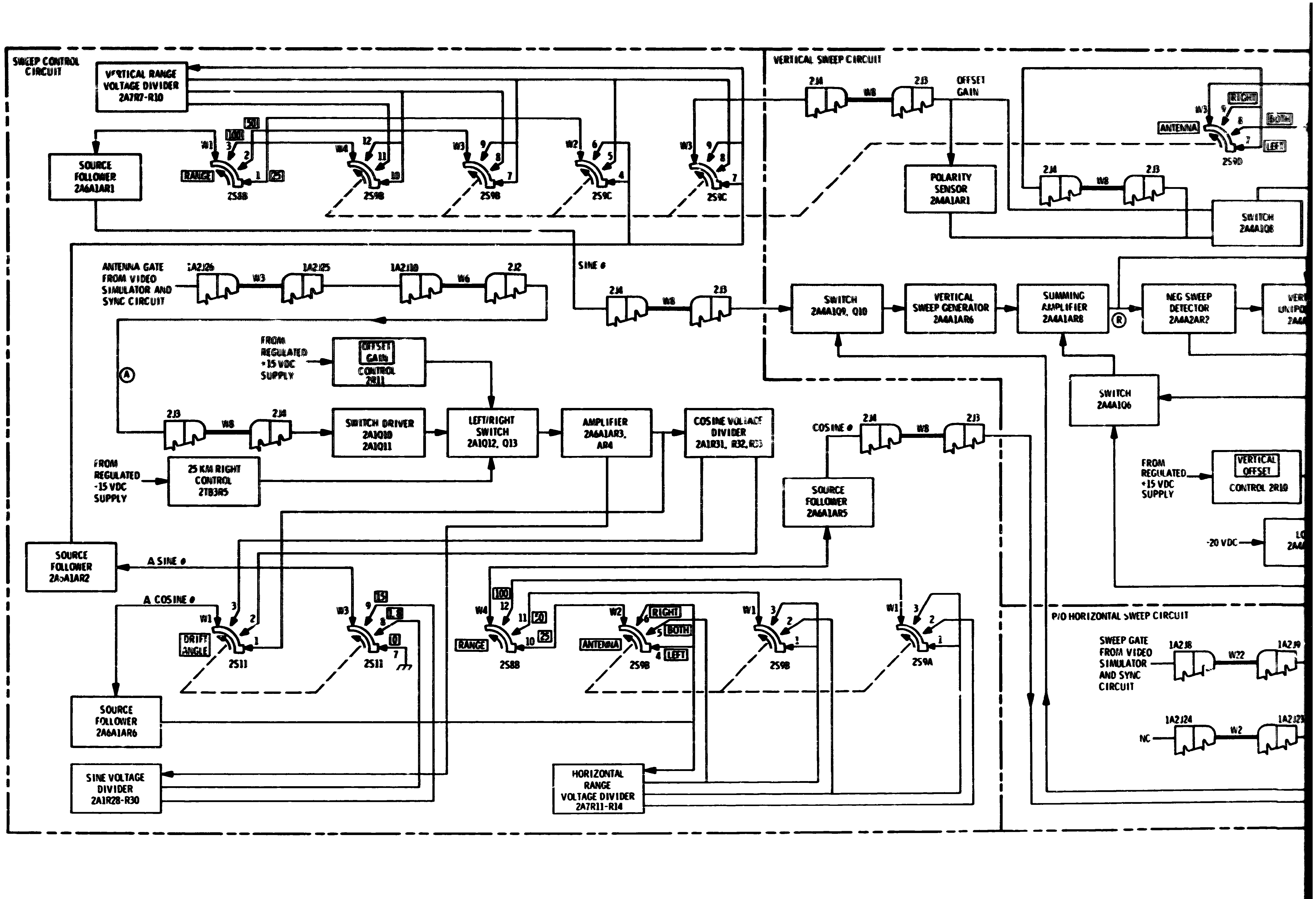
J1	LOW VOLTAGE POWER SUPPLY
J2	HIGH VOLTAGE REGULATOR
J3	HIGH VOLTAGE POWER SUPPLY

UNIT 1A2

J1	YOKE DRIVE
J2	FT VIDEO
J3	
J4	MT VIDEO
J5	
J6	TEST VIDEO
J7	
J8	SWEEP GATE
J9	
J10	RACK/SWEEP
J11	INDICATOR/SWEEP
J12	DC POWER IN
J13	AC POWER IN
J14	YOKE LOAD
J15	HIGH VOLTAGE REGULATOR
J16	HIGH VOLTAGE POWER SUPPLY
J17	RACK/NAV SIM
J18	NAV SIM/RACK
J19	RACK/ADAS
J20	ADAS/RACK
J21	RACK/I BOX
J22	I-BOX/RACK
J23	RACK/RCDR
J24	RCDR/RACK
J25	RACK/RGP
J26	RGP/RACK

UNIT 2

J1	SWEEP/INDICATOR
J2	SWEEP/RACK
J3	SWEEP/CONTROL
J4	CONTROL/SWEEP
J5	LOW VOLTAGE POWER SUPPLY



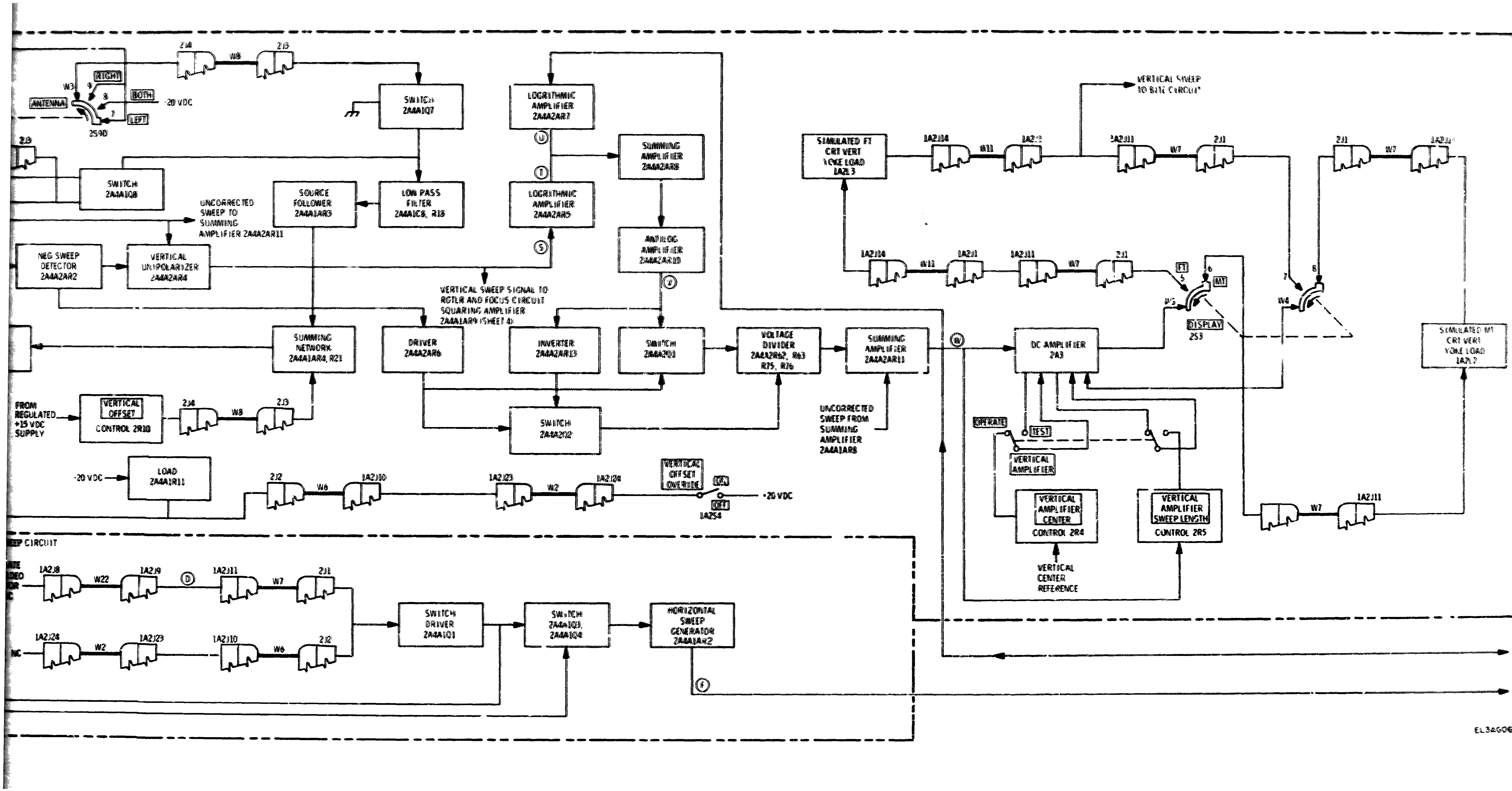
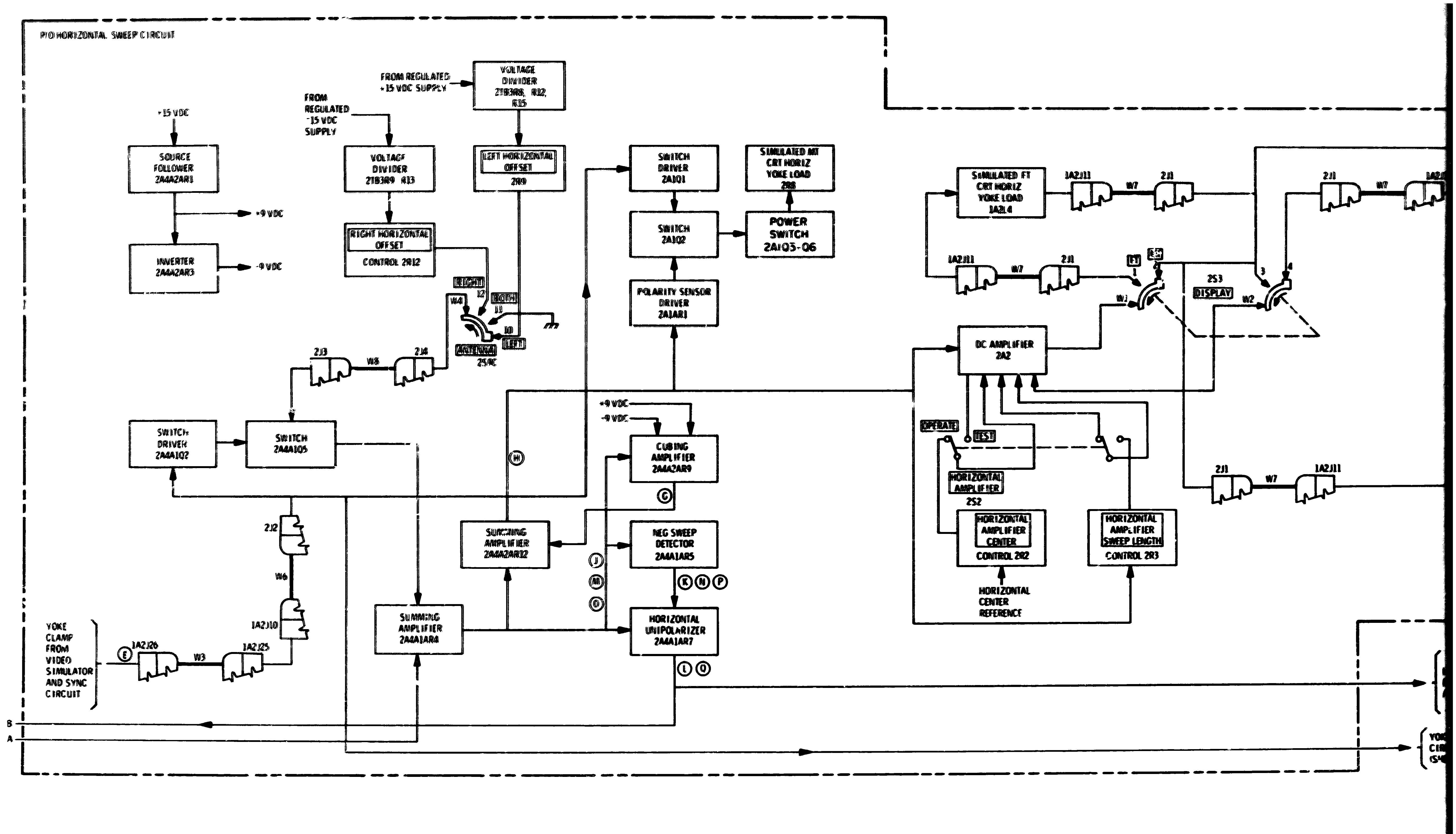
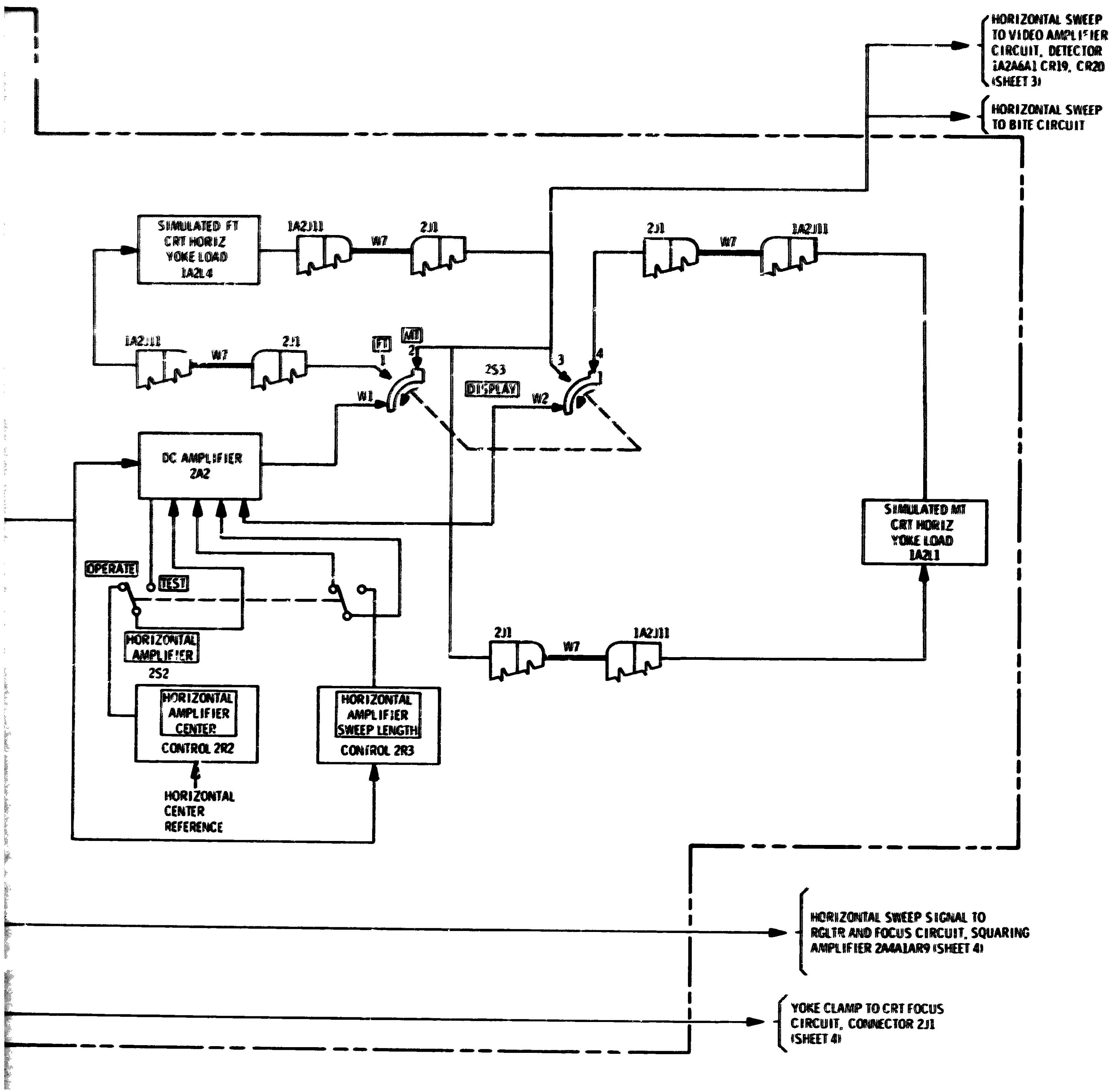


Figure FO-2. Indicating system detailed functions, block diagram (sheet 1 of 4)


P10 HORIZONTAL SWEEP CIRCUIT
+15 VDC
SOURCE FOLLOWER 2A4A2AR1
+9 VDC
INVERTER 2A4A2AR3
-9 VDC
FROM REGULATED -15 VDC SUPPLY
VOLTAGE DIVIDER 2IB3R9 R13
RIGHT HORIZONTAL OFFSET CONTROL 2R12
FROM REGULATED +15 VDC SUPPLY
VOLTAGE DIVIDER 2IB3R8, R12, R15
LEFT HORIZONTAL OFFSET 2R9
RIGHT
BOTH
LEFT
ANTENNA
2S4C
SWITCH DRIVER 2A1Q1
SWITCH 2A1Q2
POLARITY SENSOR DRIVER 2A1AR1
SIMULATED MT CRT HORIZ YOKE LOAD 2R8
POWER SWITCH 2A1Q3-Q6
SIMULATED FT CRT HORIZ YOKE LOAD 1A2L4
DC AMPLIFIER 2A2
2S3
DISPLAY
OPERATE
TEST
HORIZONTAL AMPLIFIER
2S2
HORIZONTAL AMPLIFIER CENTER CONTROL 2R2
HORIZONTAL AMPLIFIER SWEEP LENGTH CONTROL 2R3
HORIZONTAL CENTER REFERENCE
SWITCH DRIVER 2A4A1Q2
SWITCH 2A4A1Q5
CUBING AMPLIFIER 2A4A2AR9
SUMMING AMPLIFIER 2A4A2AR12
NEG SWEEP DETECTOR 2A4A1AR5
SUMMING AMPLIFIER 2A4A1AR4
HORIZONTAL UNIPOLARIZER 2A4A1AR7
YOKE CLAMP FROM VIDEO SIMULATOR AND SYNC CIRCUIT
1A2J26
W3
1A2J25
1A2J10
W6
2J2
2J3
W8
2J4
W4
1A2J11
W7
2J1
W1
W2
B
A



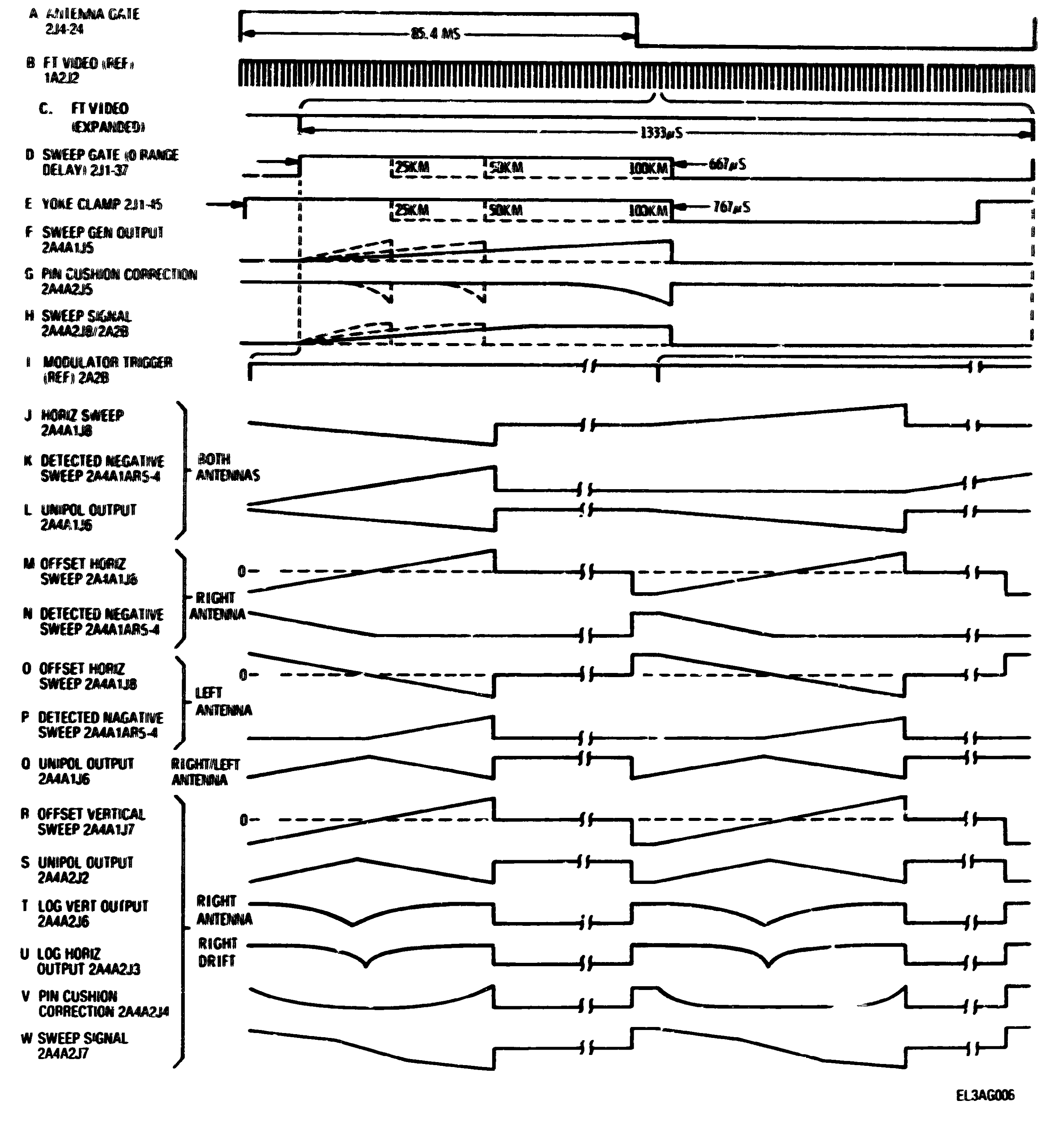
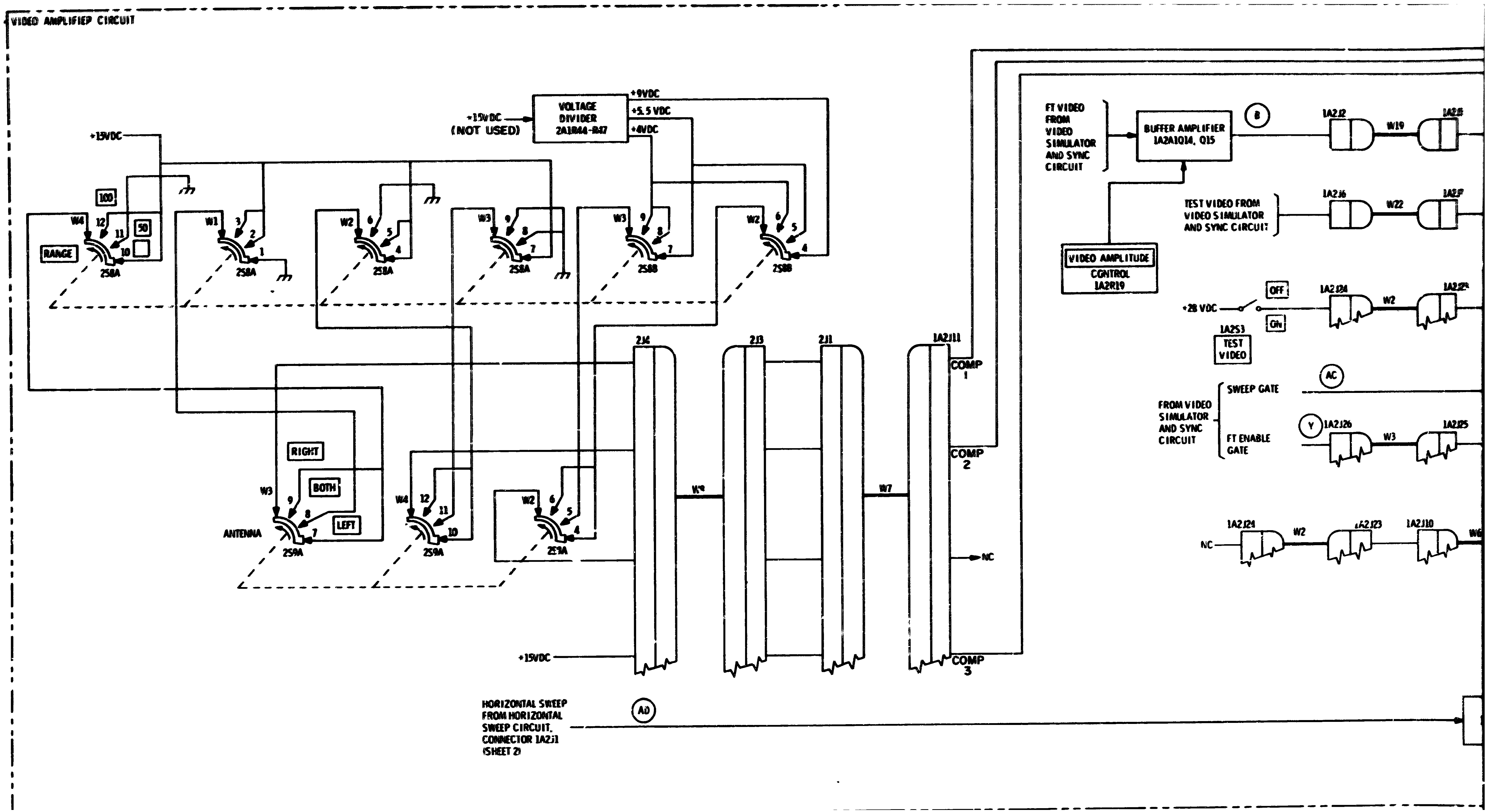


Figure FO-2. Indicating system detailed functions, block diagram (sheet 2 of 4)



VIDEO AMPLIFIER CIRCUIT
+15VDC
(NOT USED)
VOLTAGE DIVIDER 2A1R44-R47
+9VDC
+5.5 VDC
+4VDC
100
50
RANGE
2S8A
2S8B
RIGHT
BOTH
LEFT
ANTENNA
2S9A
2J4
2J3
2J1
1A2J11
COMP 1
COMP 2
COMP 3
NC
W7
FT VIDEO FROM VIDEO SIMULATOR AND SYNC CIRCUIT
BUFFER AMPLIFIER 1A2A1Q14, Q15
VIDEO AMPLITUDE CONTROL 1A2R19
TEST VIDEO FROM VIDEO SIMULATOR AND SYNC CIRCUIT
1A2J2
W19
1A2J6
W22
+28 VDC
OFF
ON
1A2S3 TEST VIDEO
1A2J34
W2
FROM VIDEO SIMULATOR AND SYNC CIRCUIT
SWEEP GATE
FT ENABLE GATE
1A2J26
W3
1A2J25
1A2J24
1A2J23
1A2J10
HORIZONTAL SWEEP FROM HORIZONTAL SWEEP CIRCUIT, CONNECTOR 1A2J1 (SHEET 2)

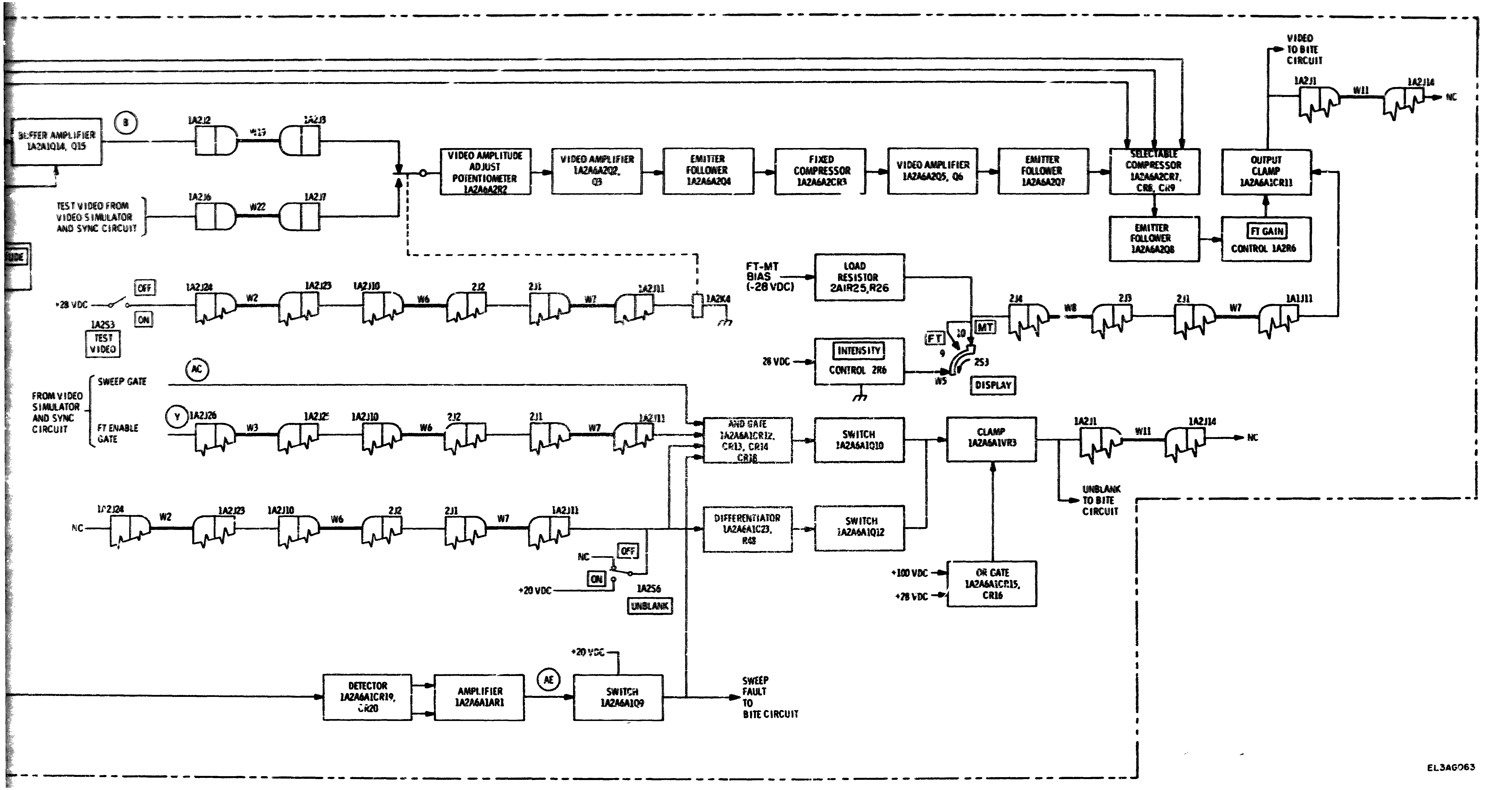


Figure FO-2. Indicating system detailed functions, block diagram (sheet 3 of 4)

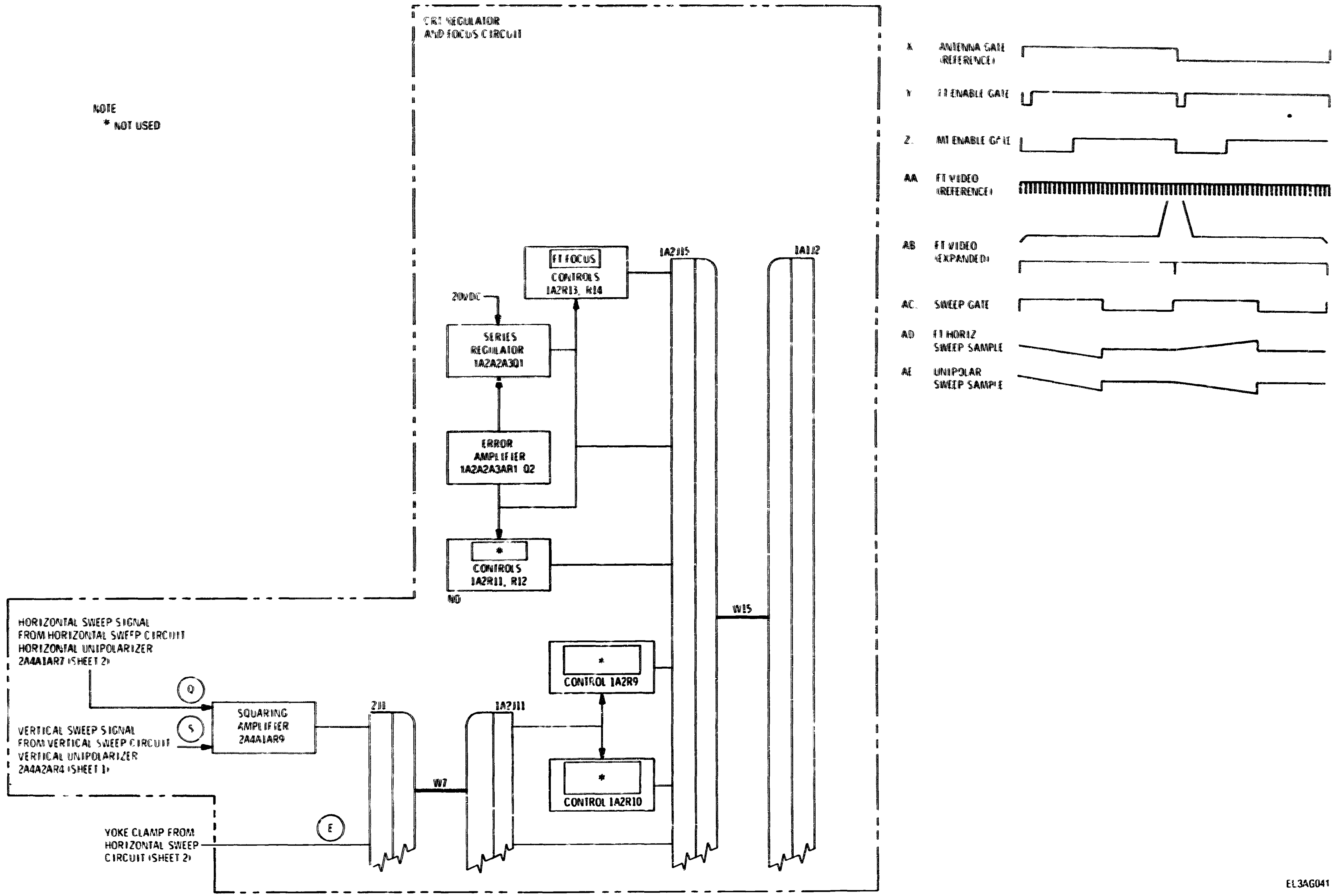
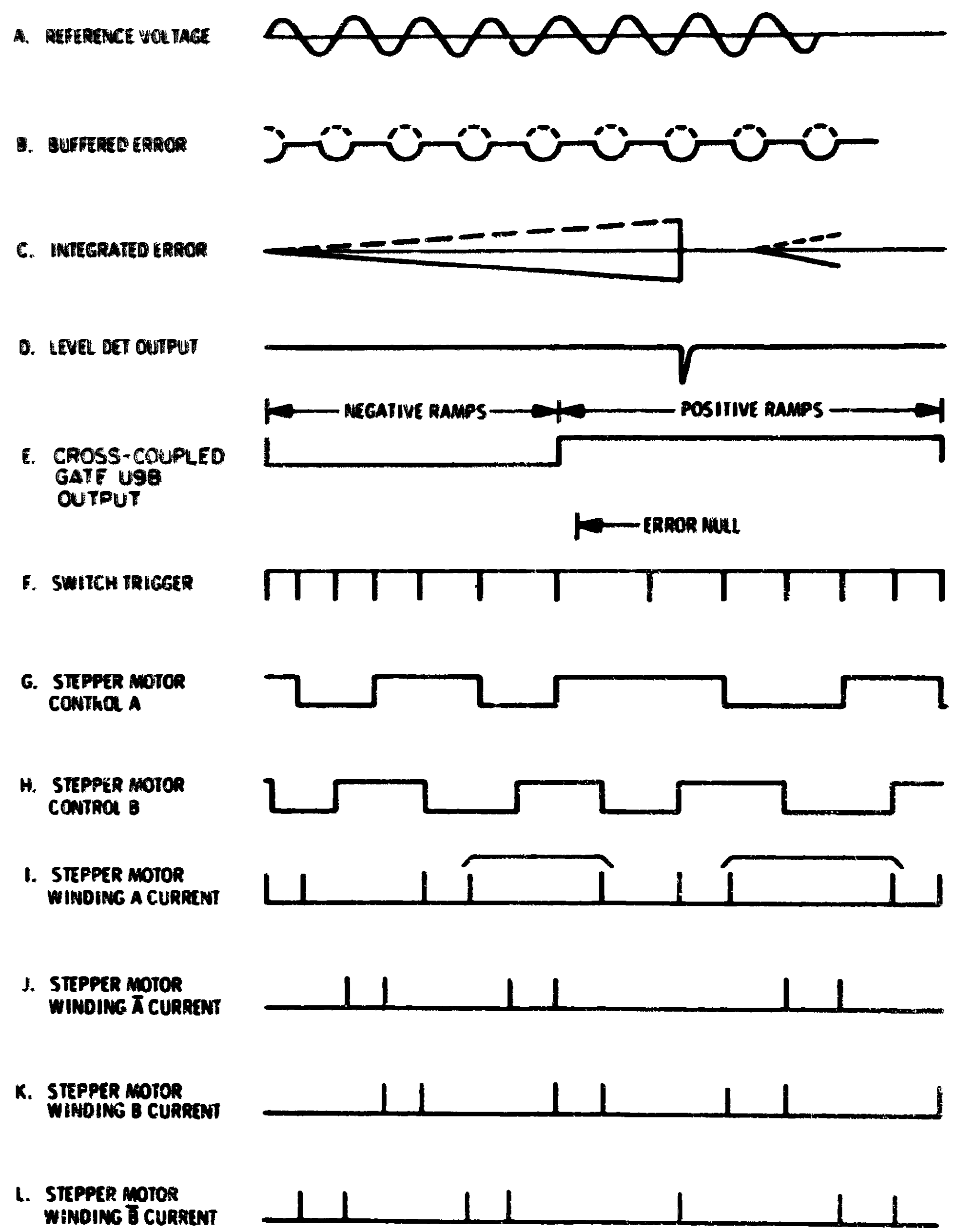
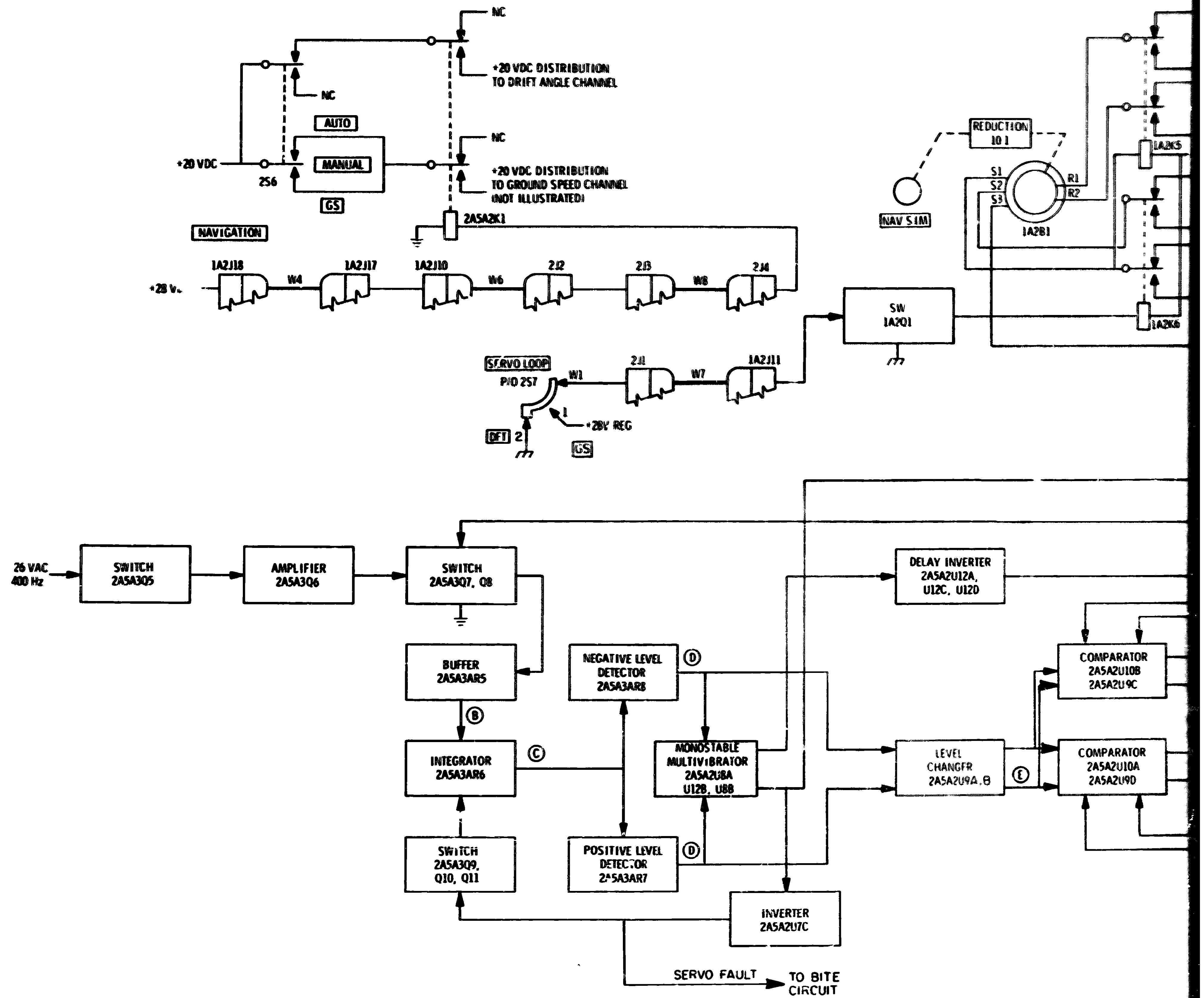


Figure FO-2. Indicating system detailed functions, block diagram (sheet 4 of 4)


A. REFERENCE VOLTAGE
B. BUFFERED ERROR
C. INTEGRATED ERROR
D. LEVEL DET OUTPUT
NEGATIVE RAMPS
POSITIVE RAMPS
E. CROSS-COUPLED GATE U9B OUTPUT
ERROR NULL
F. SWITCH TRIGGER
G. STEPPER MOTOR CONTROL A
H. STEPPER MOTOR CONTROL B
I. STEPPER MOTOR WINDING A CURRENT
J. STEPPER MOTOR WINDING Ā CURRENT
K. STEPPER MOTOR WINDING B CURRENT
L. STEPPER MOTOR WINDING B̄ CURRENT


NC
+20 VDC DISTRIBUTION TO DRIFT ANGLE CHANNEL
AUTO
MANUAL
GS
+20 VDC
2S6
+20 VDC DISTRIBUTION TO GROUND SPEED CHANNEL (NOT ILLUSTRATED)
2A5A2K1
NAVIGATION
+28 V
1A2J18
W4
1A2J17
1A2J10
W6
2J2
2J3
W8
2J4
SERVO LOOP
P/O 2S7
W1
2J1
W7
1A2J11
+28V REG
DFT
SW 1A2Q1
REDUCTION 10:1
NAV SIM
S1
S2
S3
R1
R2
1A2B1
1A2K5
1A2K6
26 VAC 400 Hz
SWITCH 2A5A3Q5
AMPLIFIER 2A5A3Q6
SWITCH 2A5A3Q7, Q8
BUFFER 2A5A3AR5
INTEGRATOR 2A5A3AR6
SWITCH 2A5A3Q9, Q10, Q11
NEGATIVE LEVEL DETECTOR 2A5A3AR8
POSITIVE LEVEL DETECTOR 2A5A3AR7
MONOSTABLE MULTIVIBRATOR 2A5A2U8A U12B, U8B
DELAY INVERTER 2A5A2U12A, U12C, U12D
LEVEL CHANGER 2A5A2U9A, B
COMPARATOR 2A5A2U10B 2A5A2U9C
COMPARATOR 2A5A2U10A 2A5A2U9D
INVERTER 2A5A2U7C
SERVO FAULT
TO BITE CIRCUIT

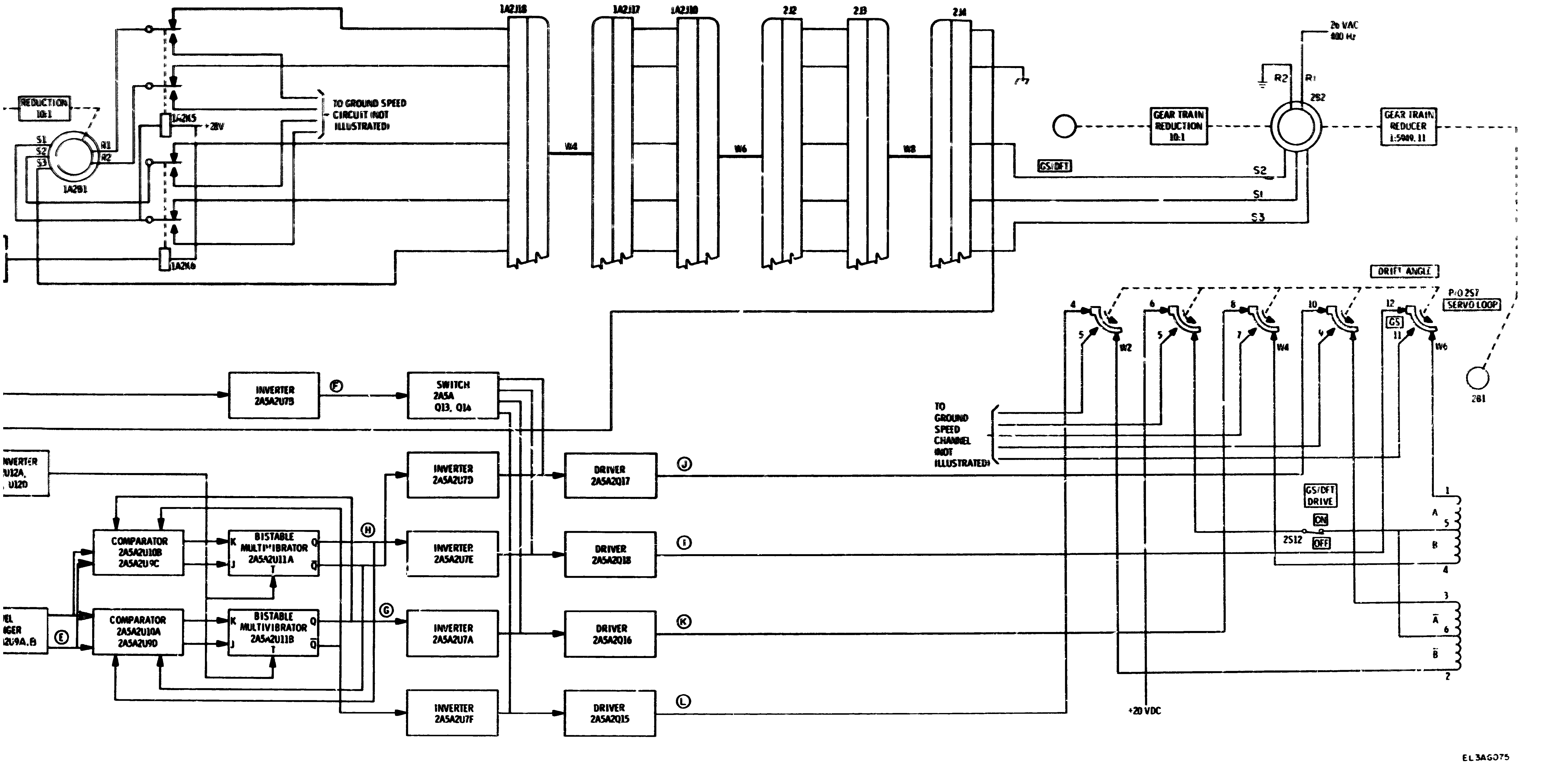
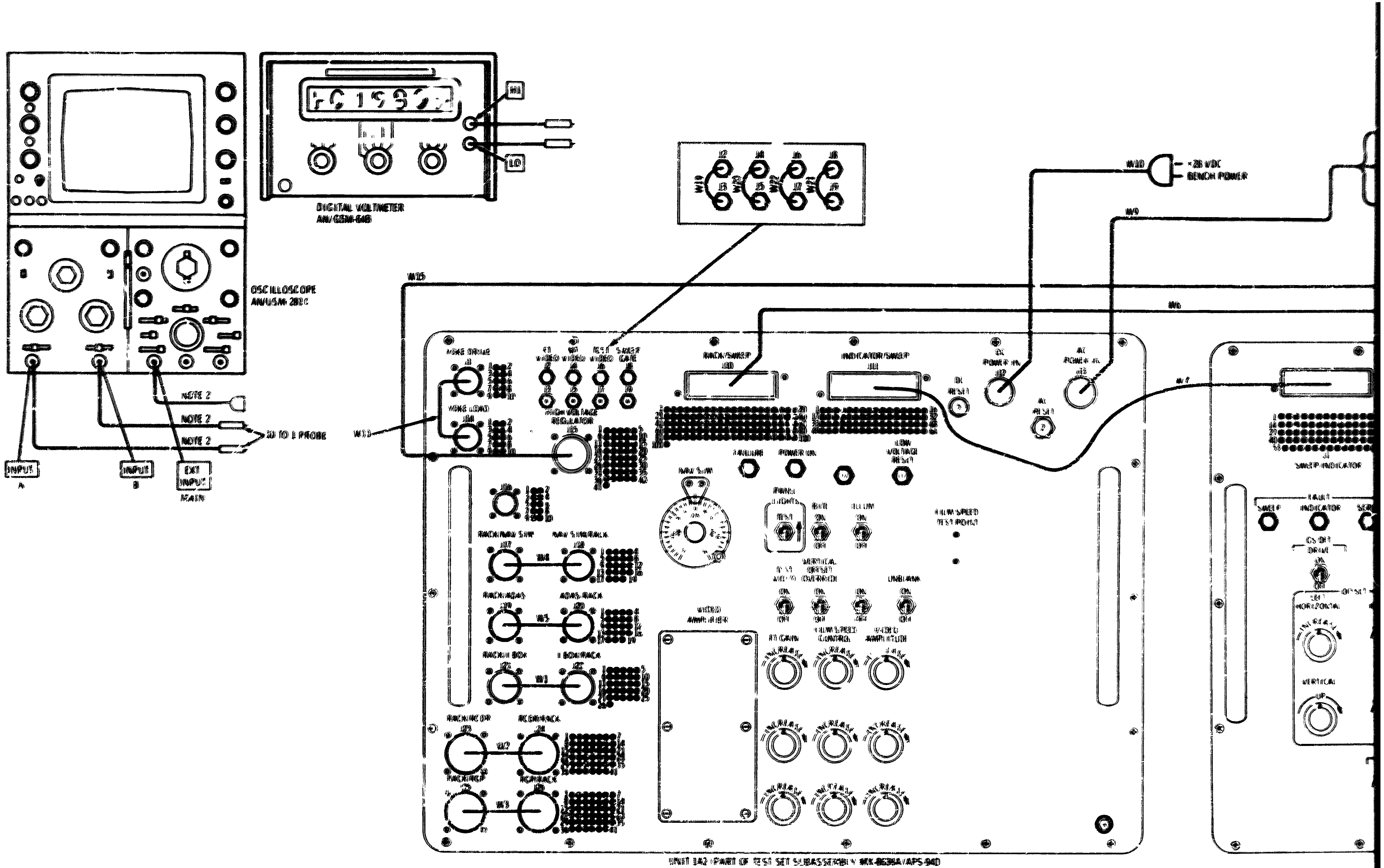


Figure FO-3. Draft angle servo loop, block diagram

NOTES

1. CABLES W1 THROUGH W11, W15, W17, W19 THROUGH W22 AND W28 ARE PART OF TEST SET SUBASSEMBLY MX-8638/APS-94D
2. CABLES ARE PART OF OSCILLOSCOPE AN/USM-281A.
3. ▭ INDICATES EQUIPMENT MARKING.



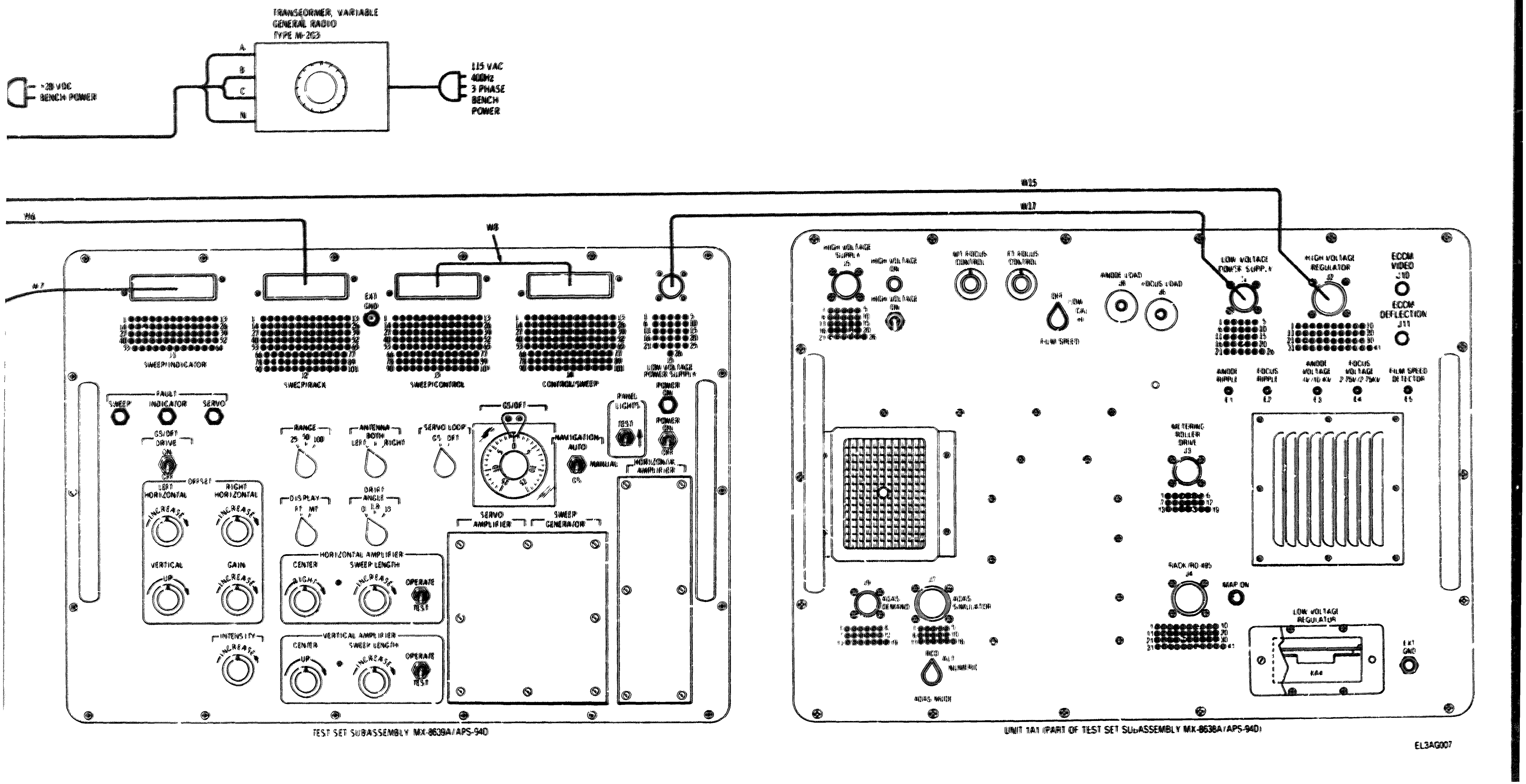
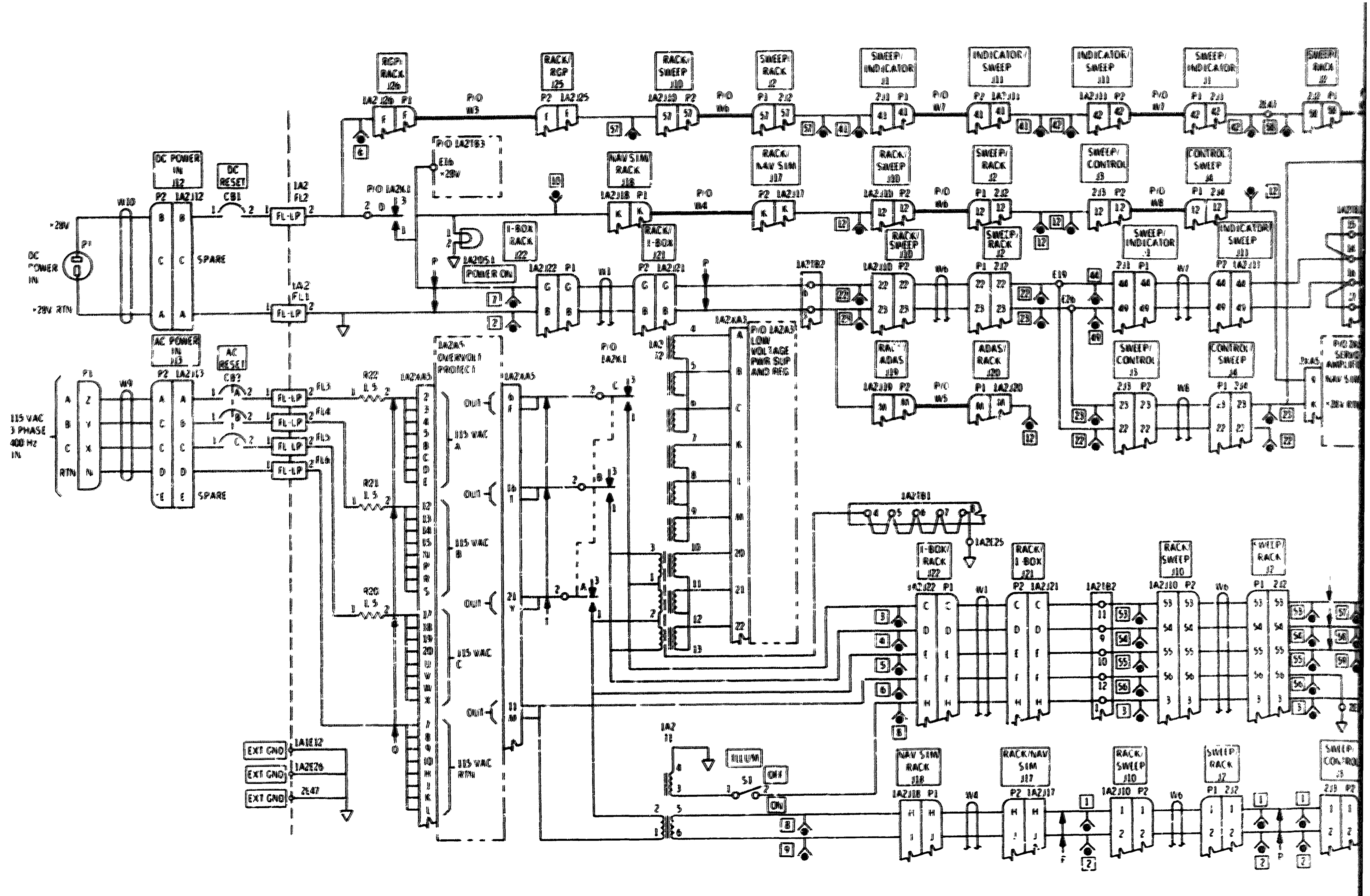


Figure FO-4. Test set group, band test setup

NOTE [ ] INDICATES EQUIPMENT MARKING

* NOT USED



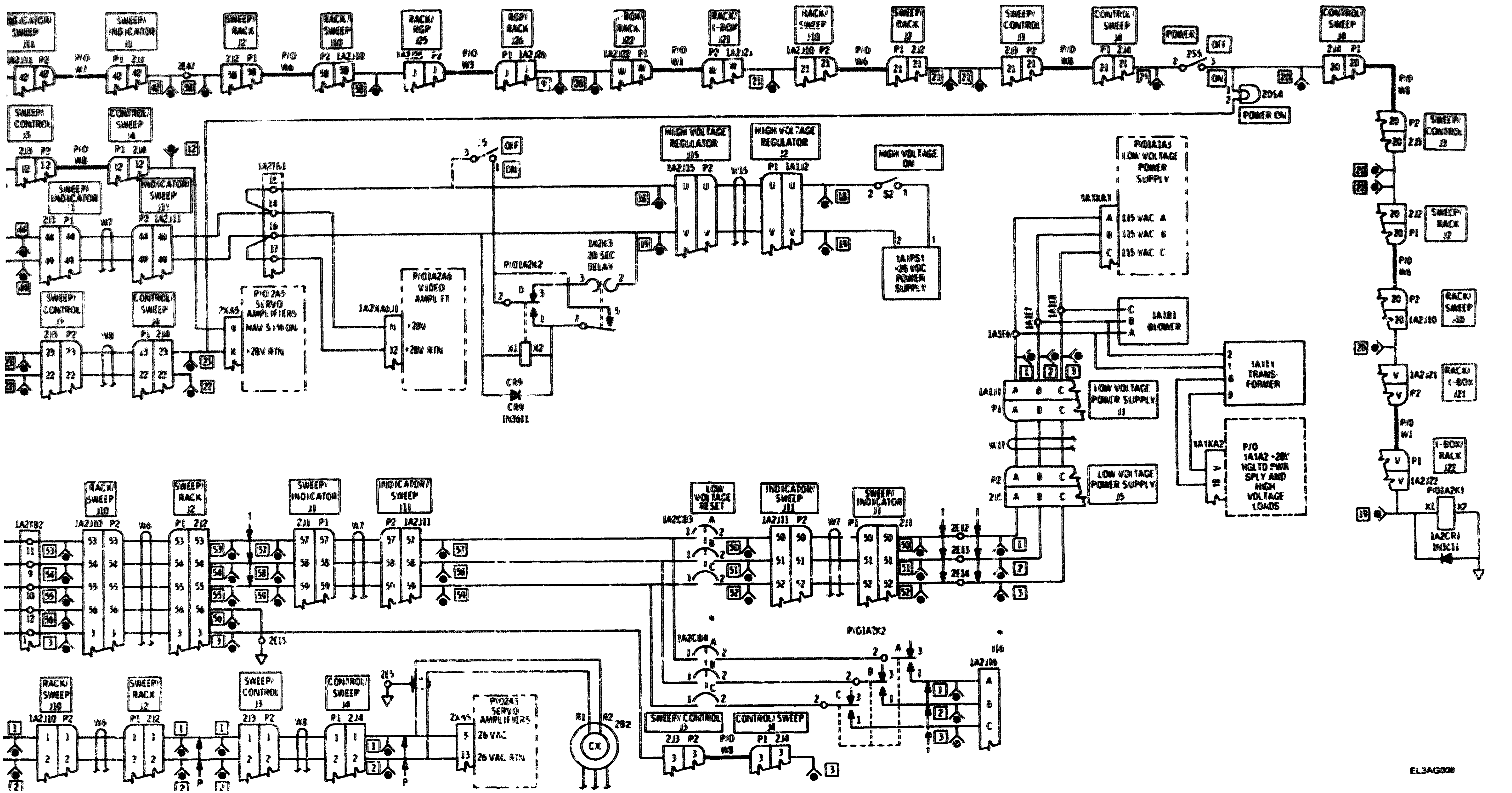


Figure FO-5. Primary power distribution and control diagram

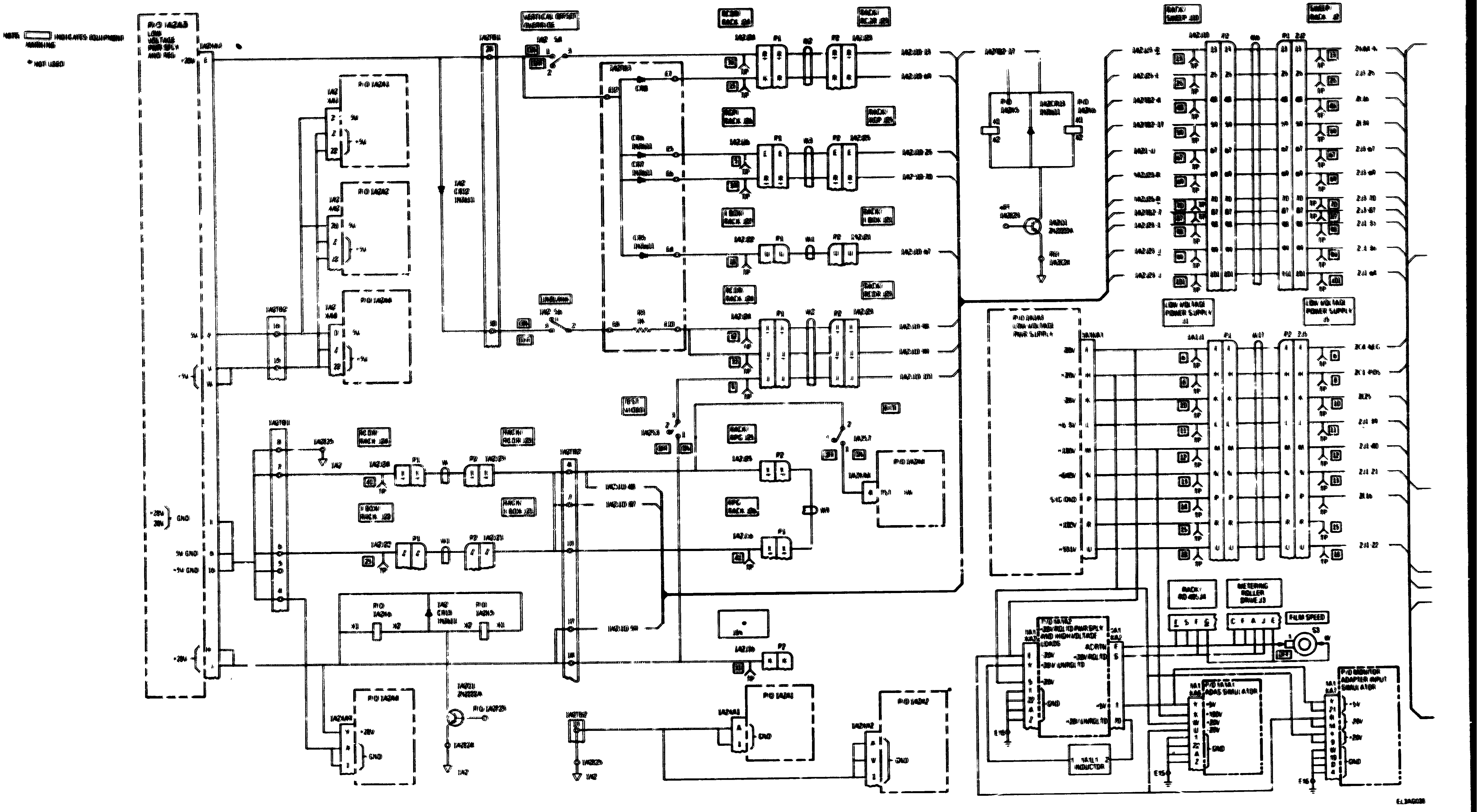


Figure FO-6. Secondary power distribution and control circuit diagram (sheet 1 of 3)

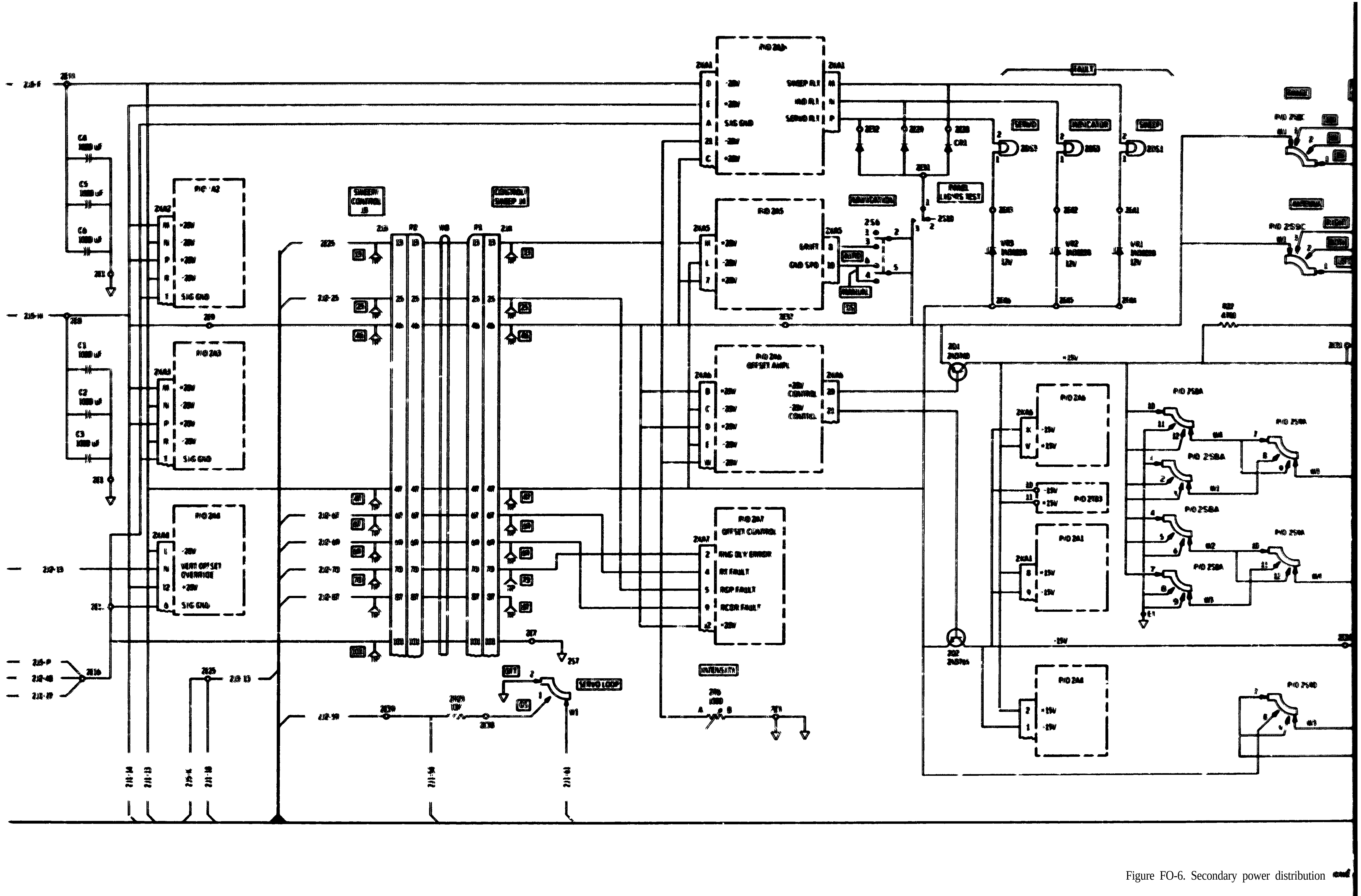


Figure FO-6. Secondary power distribution

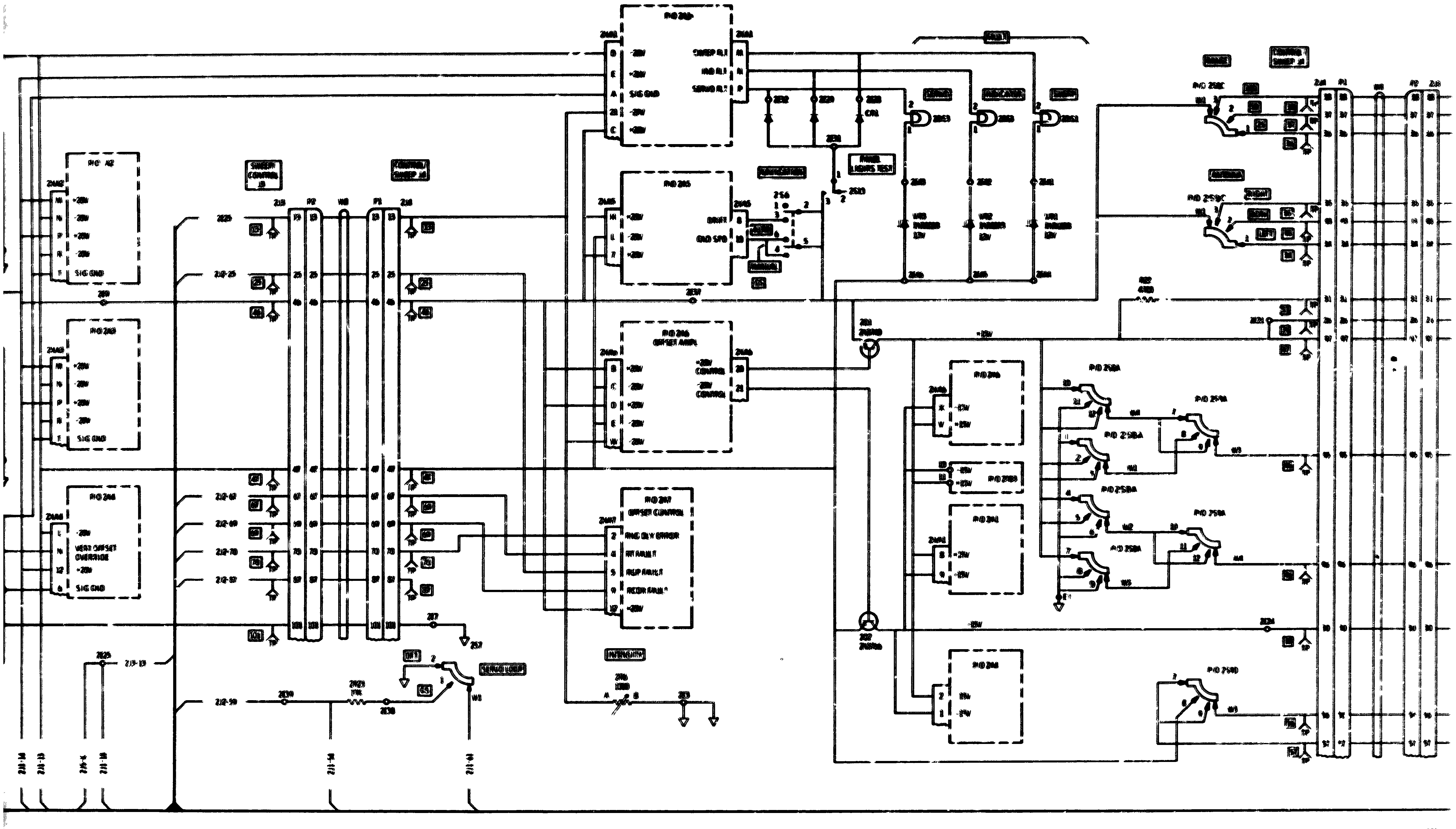


Figure FO-6 Secondary power distribution and control circuit diagram (sheet 2 of 8)

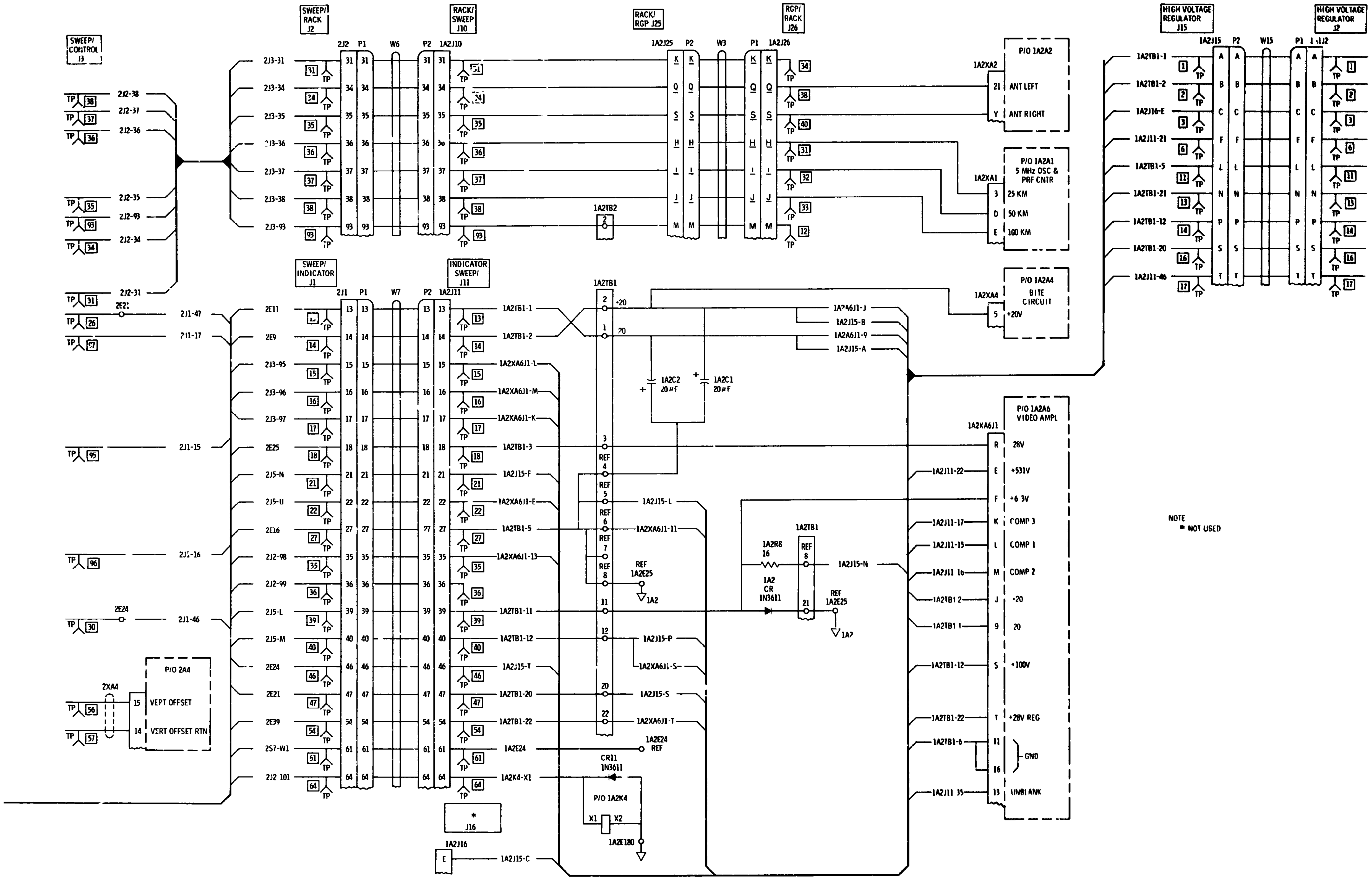


Figure FO-6. Secondary power distribution and control circuit diagram (sheet 3 of 3)

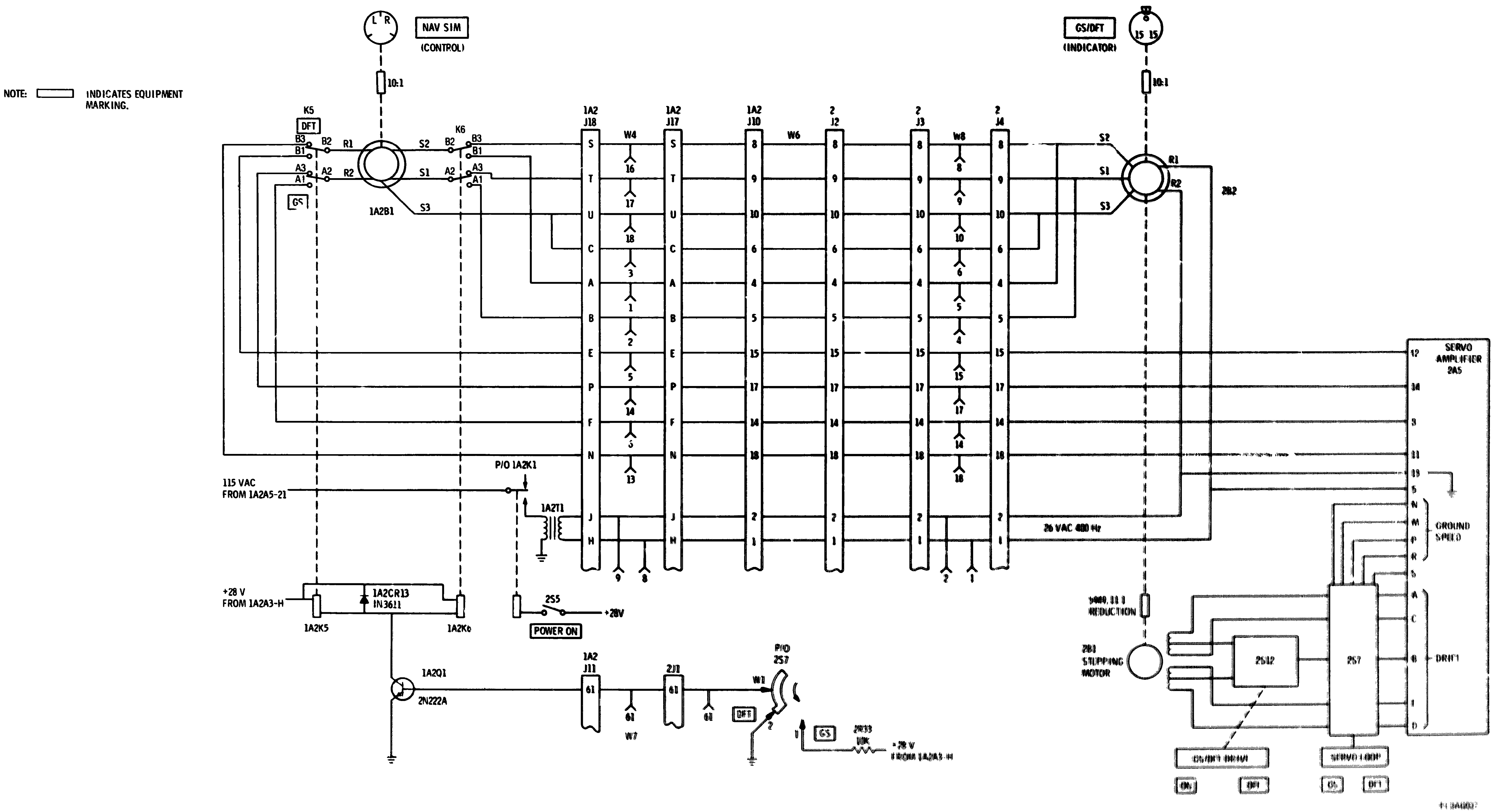
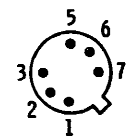


Figure FO-7. Servo loop simplified wiring diagram

NOTES:

1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN FOR COMPLETE DESIGNATIONS PREFIX WITH 2.
2. UNLESS OTHERWISE SPECIFIED: ALL RESISTORS ARE IN OHMS. ALL CAPACITORS ARE IN μF.
3. SEMICONDUCTOR DEVICES A6A1Q4 AND A6A1Q2 PIN ORIENTATION IS AS SHOWN BELOW.



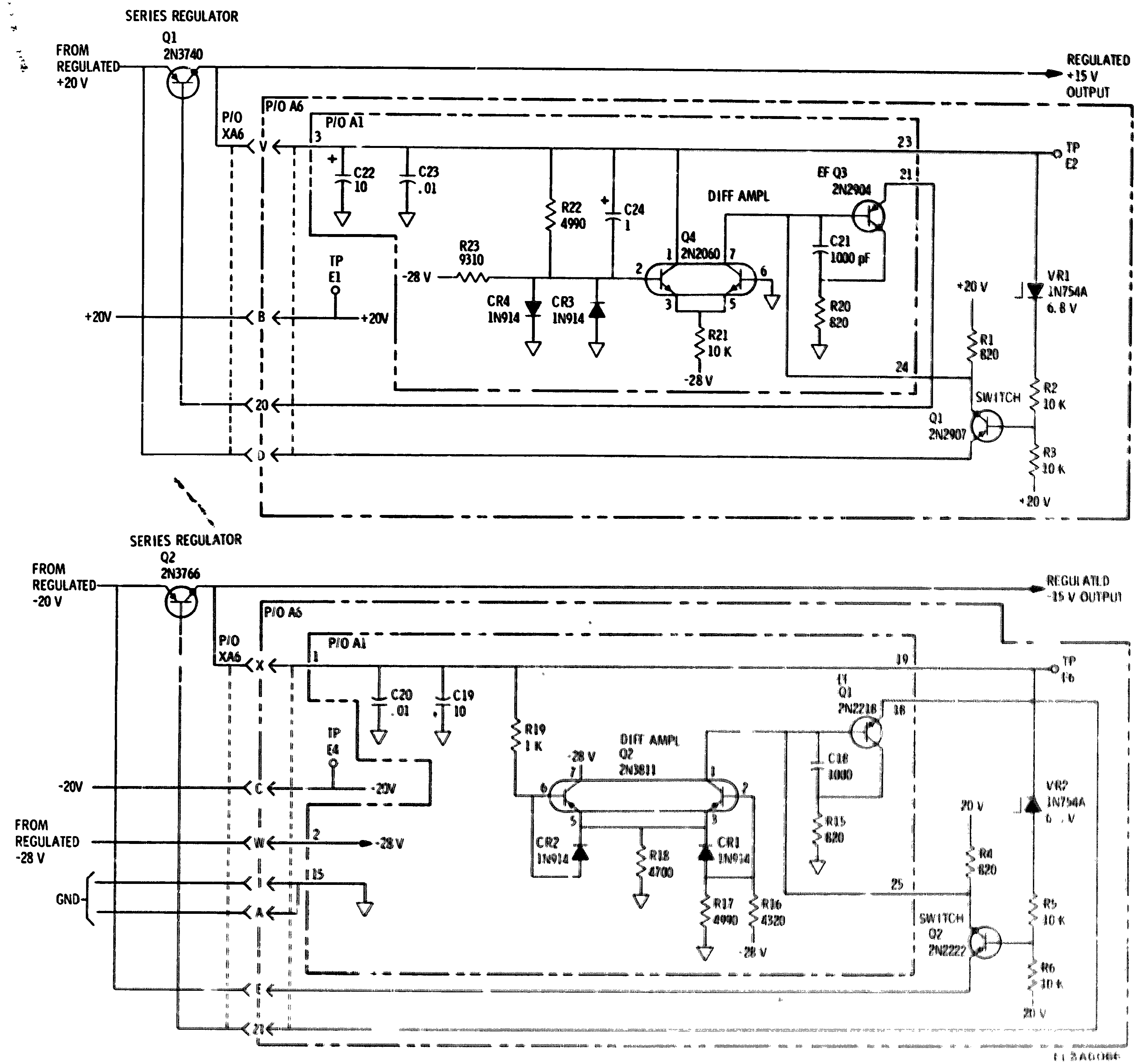
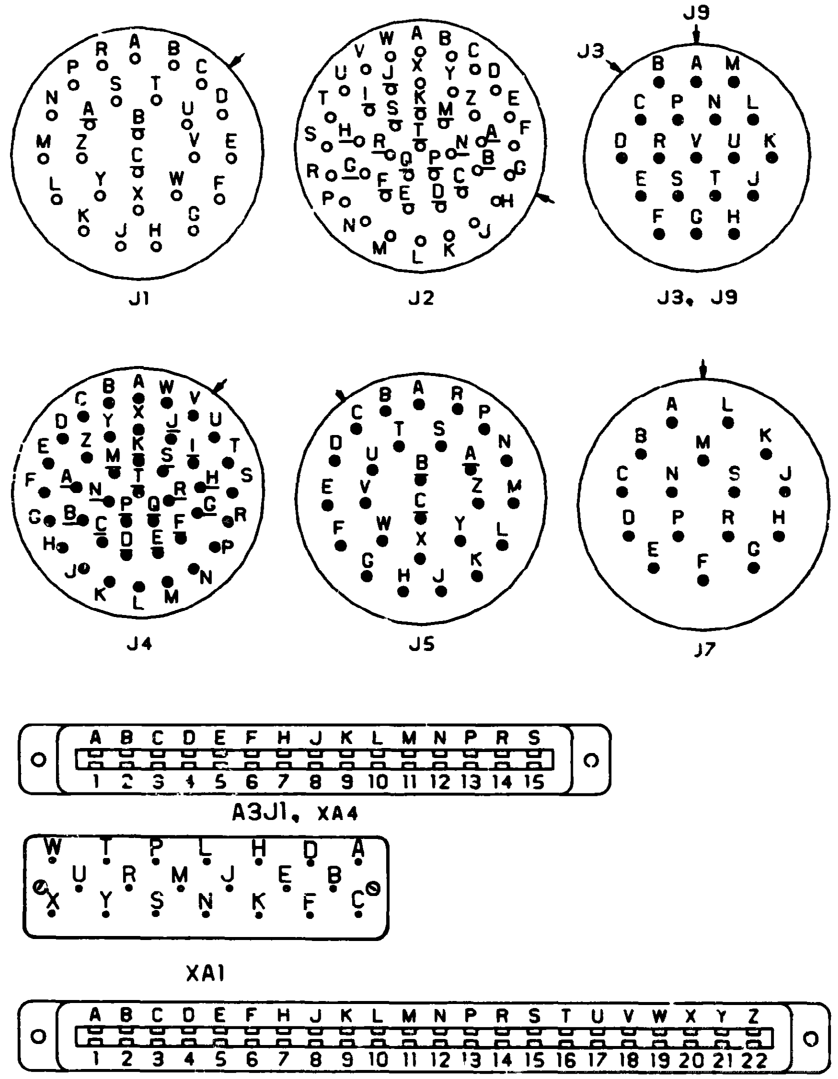
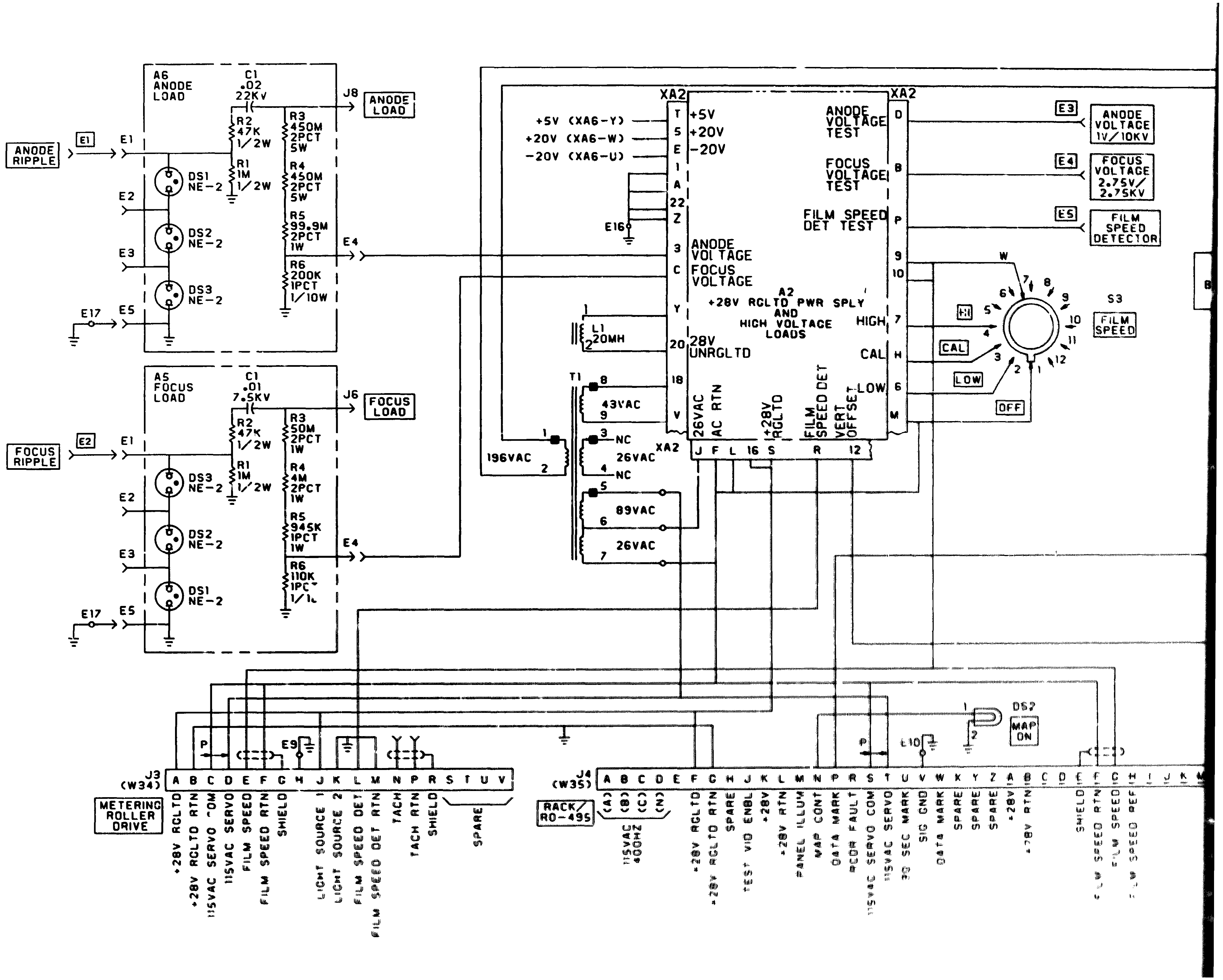


Figure FO-8. Fifteen-volt power supplies functional schematic

NOTES:

1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. FOR COMPLETE DESIGNATIONS PREFIX WITH 1A1.
2. UNLESS OTHERWISE SPECIFIED: ALL RESISTORS ARE IN OHMS. ALL VOLTAGES ARE DC.
3. ▭ INDICATES EQUIPMENT MARKINGS.
4. CONNECTOR PIN ORIENTATIONS ARE AS SHOWN BELOW (VIEWED FROM MATING SIDE).





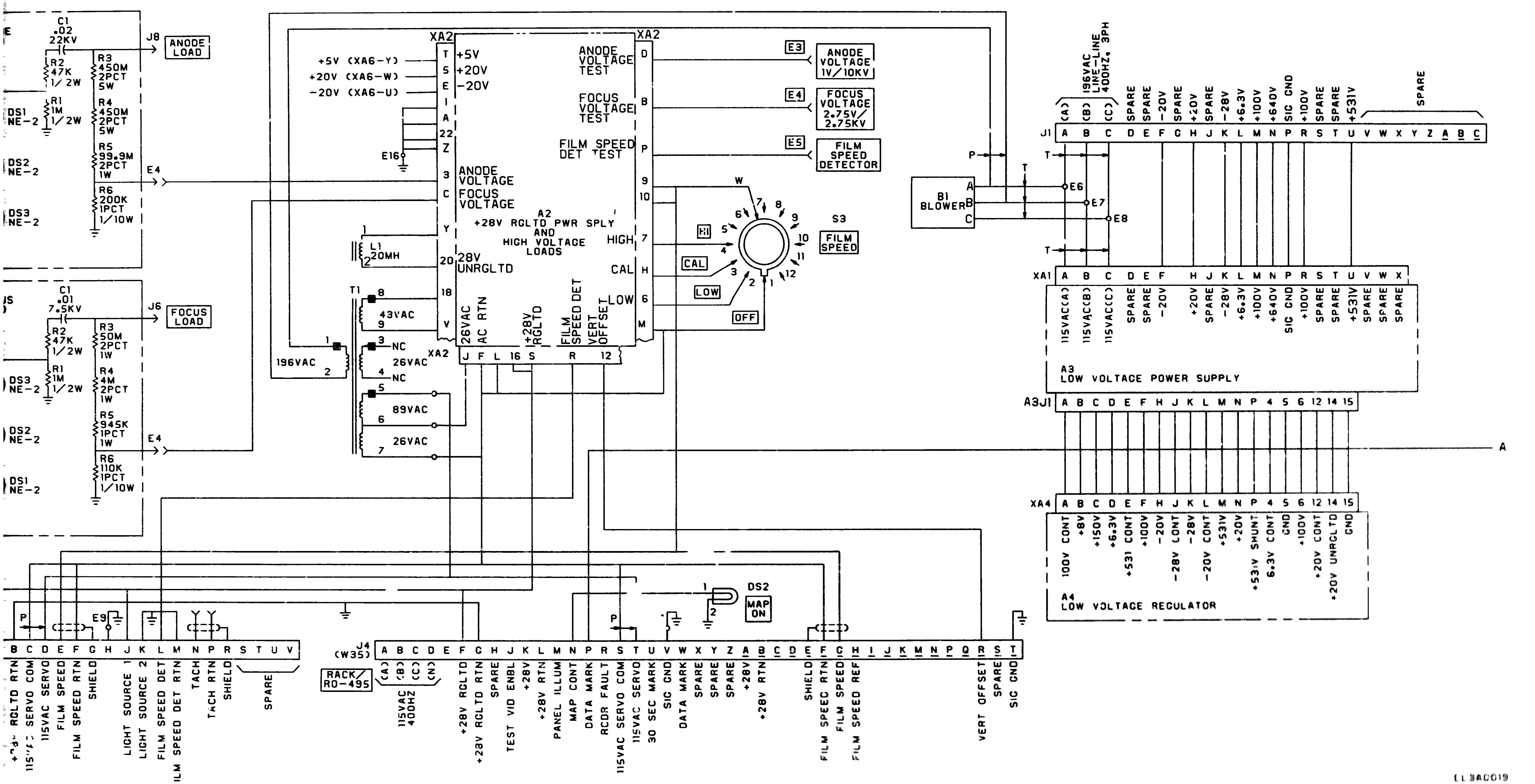


Figure FO-9. Test Set Subassembly MX-8638A/APS-94D Unit 1A1, interconnection diagram (sheet 1 of 2)

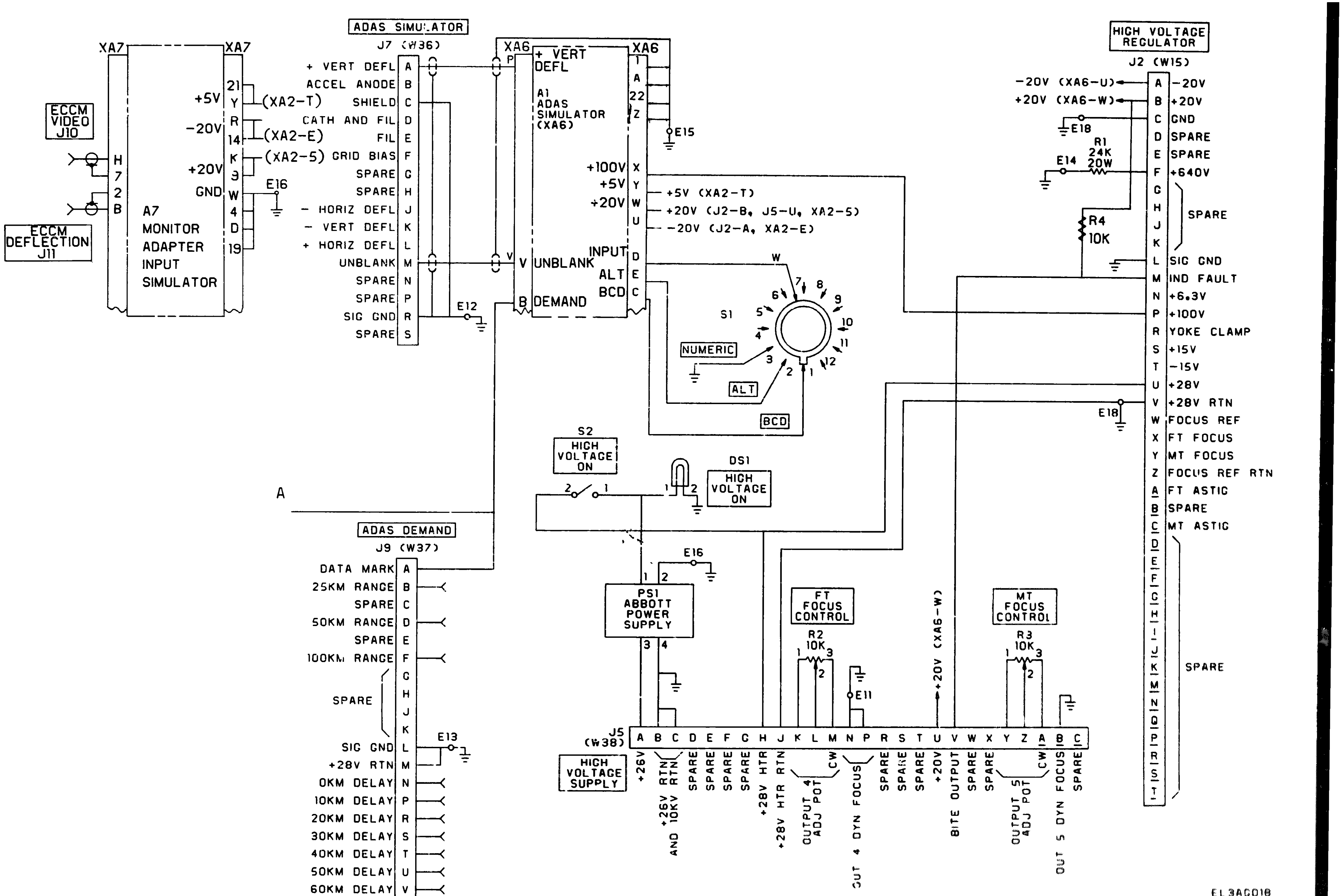


Figure FO-9. Test Set Subassembly MX-8638A/APS-94D, Unit 1A1, interconnection diagram (sheet 2 of 2)

NOTES:

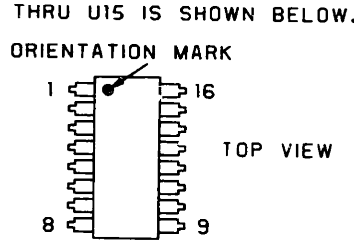
1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. FOR COMPLETE DESIGNATION PREFIX WITH 1A1A1.

2. UNLESS OTHERWISE SPECIFIED:
ALL RESISTORS ARE IN OHMS, ±5 PCT, 1/4 WATT.
ALL CAPACITORS ARE IN UF.
ALL VOLTAGES ARE IN DC.

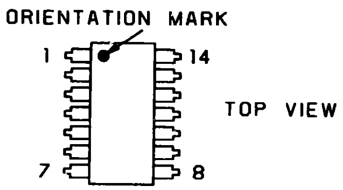
3. INTEGRATED CIRCUIT DEVICES ARE IDENTIFIED ON THE DRAWING BY THE UNDERLINED PORTION OF THE TYPE NUMBER LISTED BELOW. VOLTAGE AND GROUND PINS, PINS WITH NO INTERNAL CONNECTION (NC) AND SPARES (IN PARENTHESIS) ARE INDICATED.

REF DES	TYPE NUMBER	+5V PIN	GND PIN	NO INTERNAL CONNECTION AND SPARE PINS
U1	MC14528B	16	8	
U2	MC4324	14	7	(8,10,11,12,13)
U3	MC14024	14	7	
U4	MC14011	14	7	
U5	MC14069	14	7	
U6	MC14017	16	8	
U7	MC14017	16	8	
U8	MC14017	16	8	
U9	MC14023	14	7	
U10	MC14163B	16	8	
U11	MC14044B	16	8	
U12	MC14528B	16	8	
U13	MC14040B	16	8	
U14	51-P06640F001	16	8	
U15	MC14512	16	8	
U16	MC14001	14	7	(1,2,3)
U17	MC14013B	14	7	
U18	MC14011	14	7	

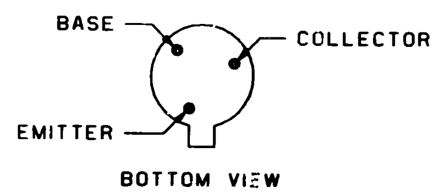
PIN ORIENTATION FOR INTEGRATED CIRCUIT DEVICES U1, U6, AND U10 THRU U15 IS SHOWN BELOW.



5. PIN ORIENTATION FOR INTEGRATED CIRCUIT DEVICES U3 THRU U5, U9, U16, AND U17 IS SHOWN BELOW.



6. PIN ORIENTATION FOR SEMICONDUCTOR DEVICES Q1 THRU Q11 IS SHOWN BELOW.



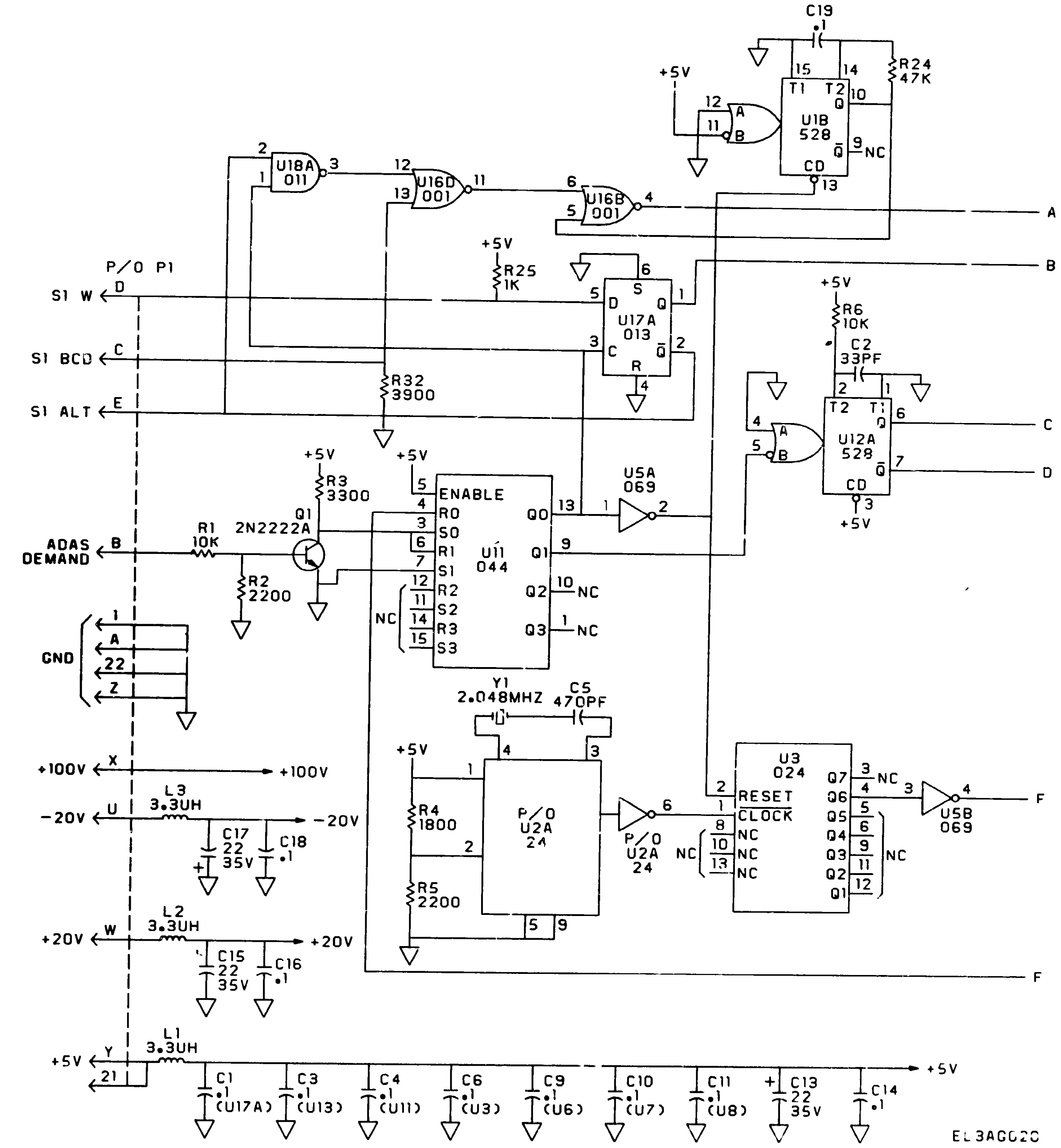
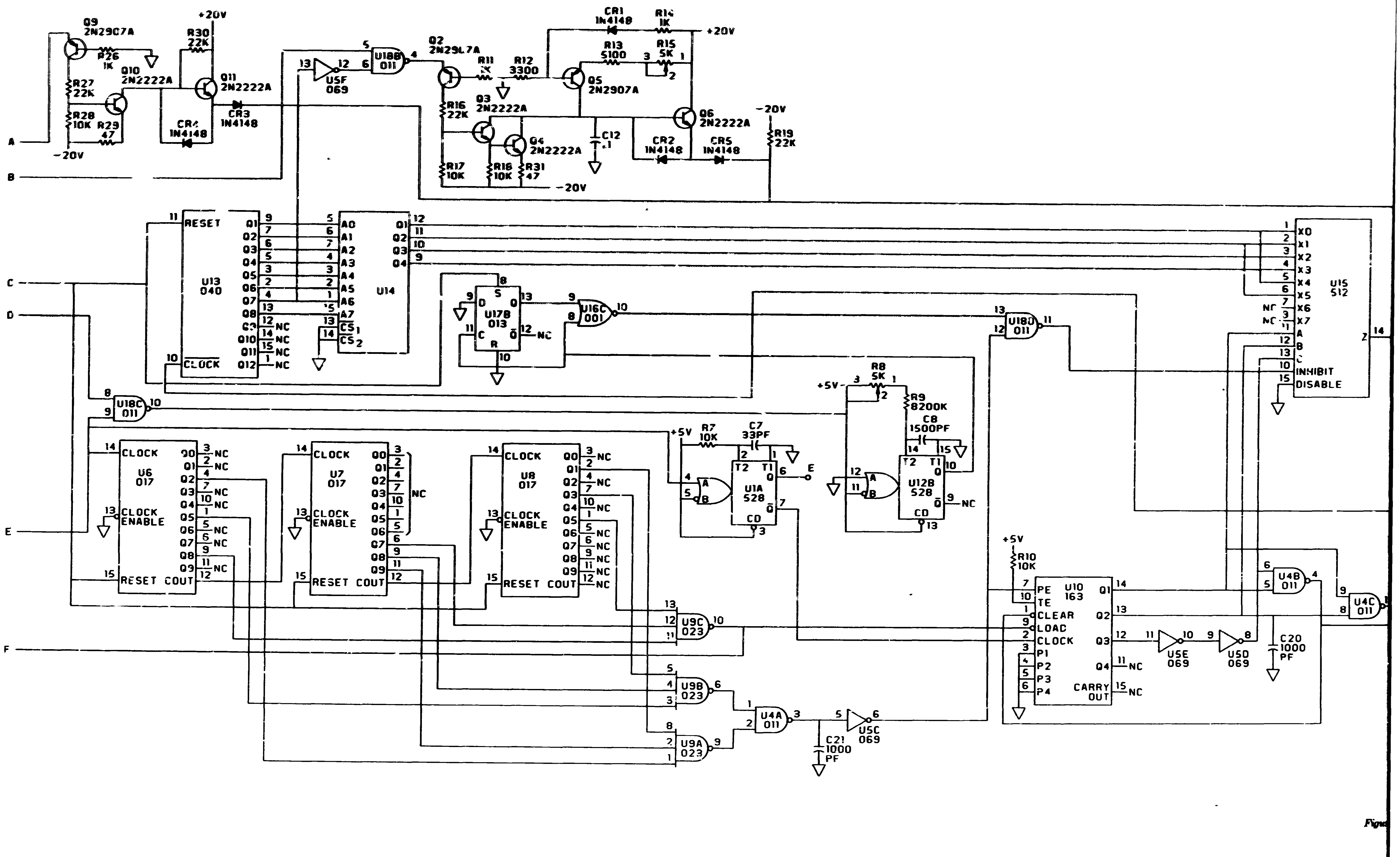


Figure FO-10. ADAS Simulator module 1A1A1, schematic diagram (sheet 1 of 2)



Q9 2N2907A
R26 1K
R27 22K
Q10 2N2222A
R28 10K
R29 47
-20V
+20V
R30 22K
Q11 2N2222A
CR4 1N4148
CR3 1N4148
U5F 069
U18B 011
Q2 2N29L7A
R11 1K
R12 3300
R16 22K
Q3 2N2222A
Q4 2N2222A
R17 10K
R18 10K
R31 47
-20V
CR1 1N4148
R14 1K
+20V
R13 5100
R15 5K
Q5 2N2907A
C12 .1
Q6 2N2222A
CR2 1N4148
CR5 1N4148
-20V
R19 22K
A
B
C
D
E
F
RESET
U13 040
CLOCK
U14
A0 A1 A2 A3 A4 A5 A6 A7
CS1 CS2
U17B 013
U16C 001
U18D 011
U15 512
X0 X1 X2 X3 X4 X5 X6 X7
INHIBIT
DISABLE
U18C 011
+5V
R8 5K
R9 8200K
C8 1500PF
R7 10K
C7 33PF
U1A 528
U12B 528
CLOCK
U6 017
CLOCK ENABLE
RESET COUT
U7 017
U8 017
U9C 023
U9B 023
U9A 023
U4A 011
C21 1000 PF
U5C 069
+5V
R10 10K
U10 163
PE TE CLEAR LOAD CLOCK
P1 P2 P3 P4
CARRY OUT
U5E 069
U5D 069
C20 1000 PF
U4B 011
U4C 011
NC

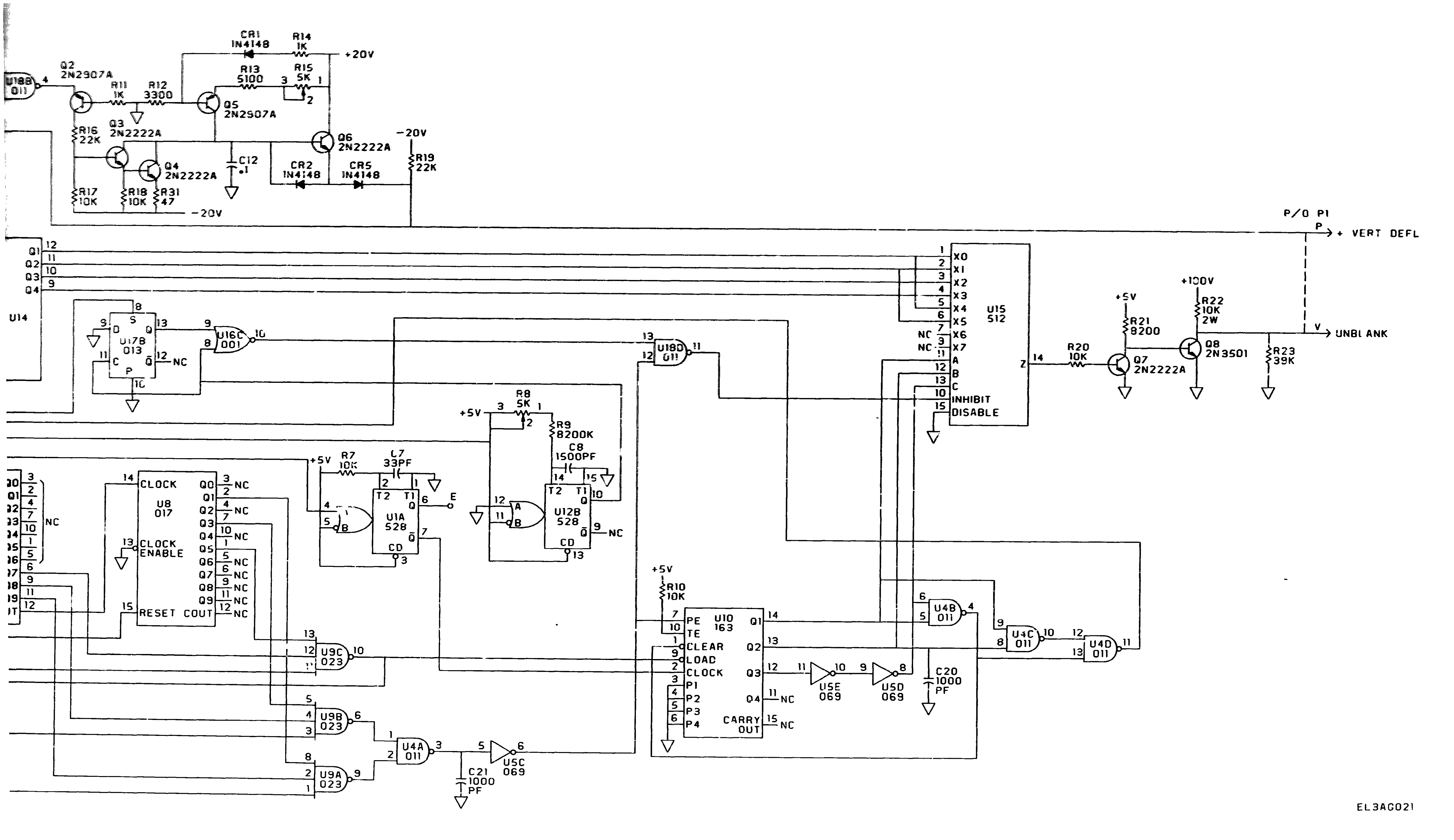


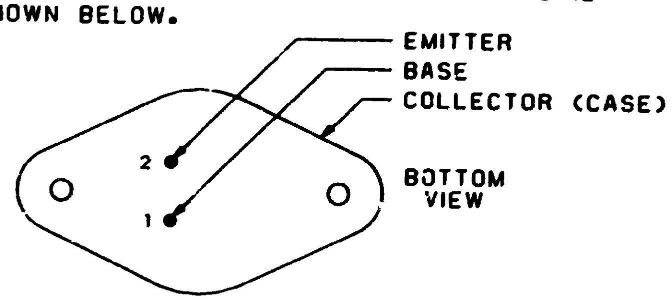
Figure FO-10. ADAS Simulator module 1A1A1, schematic diagram (sheet 2 of 2)

NOTES:

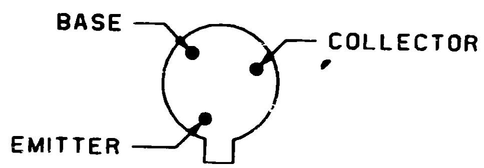
1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. FOR COMPLETE DESIGNATION PREFIX WITH 1A1A2.

2. UNLESS OTHERWISE SPECIFIED:
   ALL RESISISTORS ARE IN OHMS, ±5PCT, 1/4 WATT.
   ALL CAPACITORS ARE IN UF.
   ALL INDUCTORS ARE IN UH.
   ALL VOLTAGES ARE DC.

3. PIN ORIENTATION FOR TRANSISTOR TYPE 2N3715 IS SHOWN BELOW.

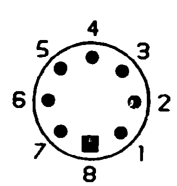


4. PIN ORIENTATION FOR TRANSISTOR TYPE 2N2907 IS SHOWN BELOW.



BOTTOM VIEW

5. PIN ORIENTATION FOR INTEGRATED CIRCUIT HA2-2600-2 IS SHOWN BELOW.



BOTTOM VIEW

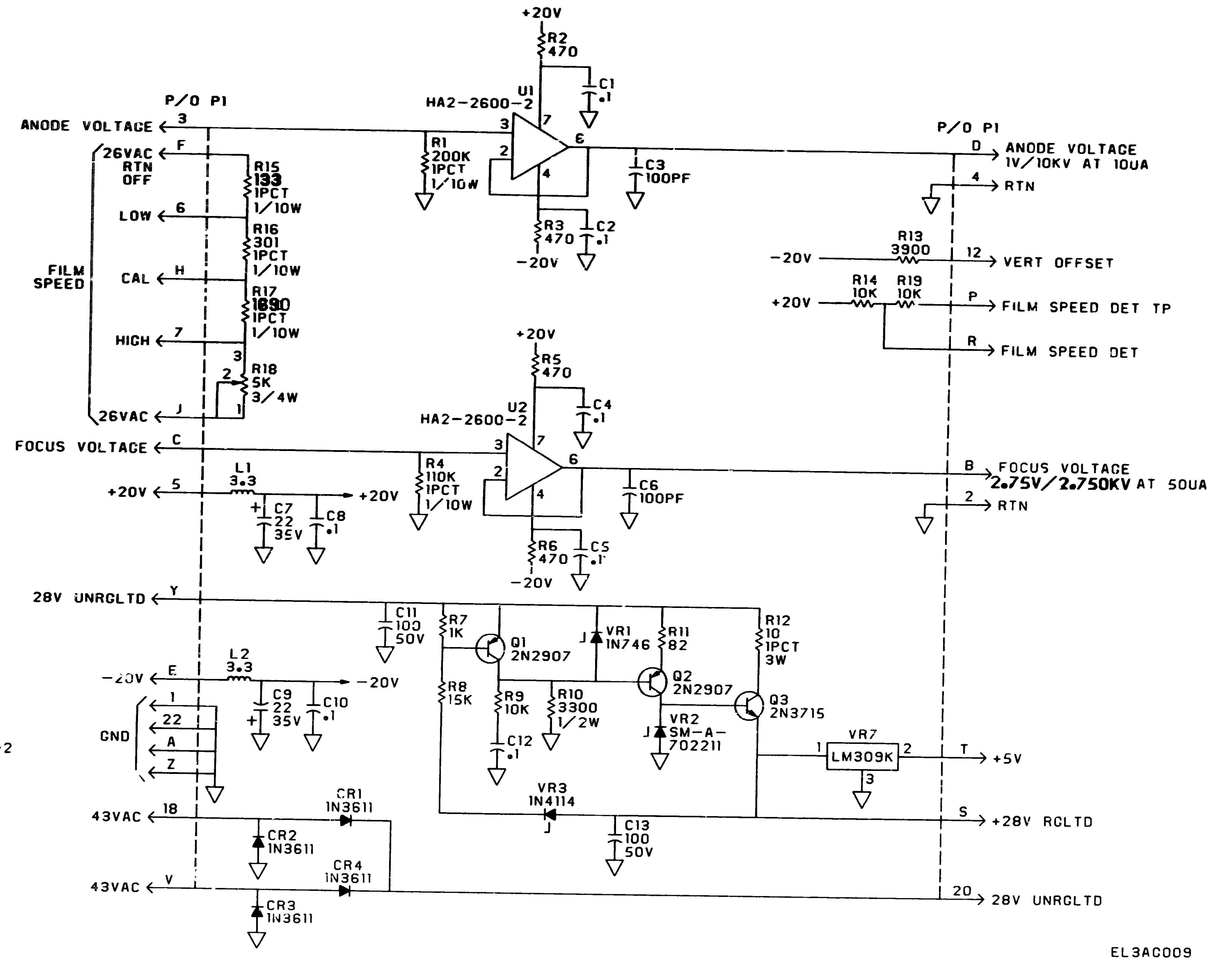


Figure FO-11. Regulated +28-volt power supply and high voltage loads

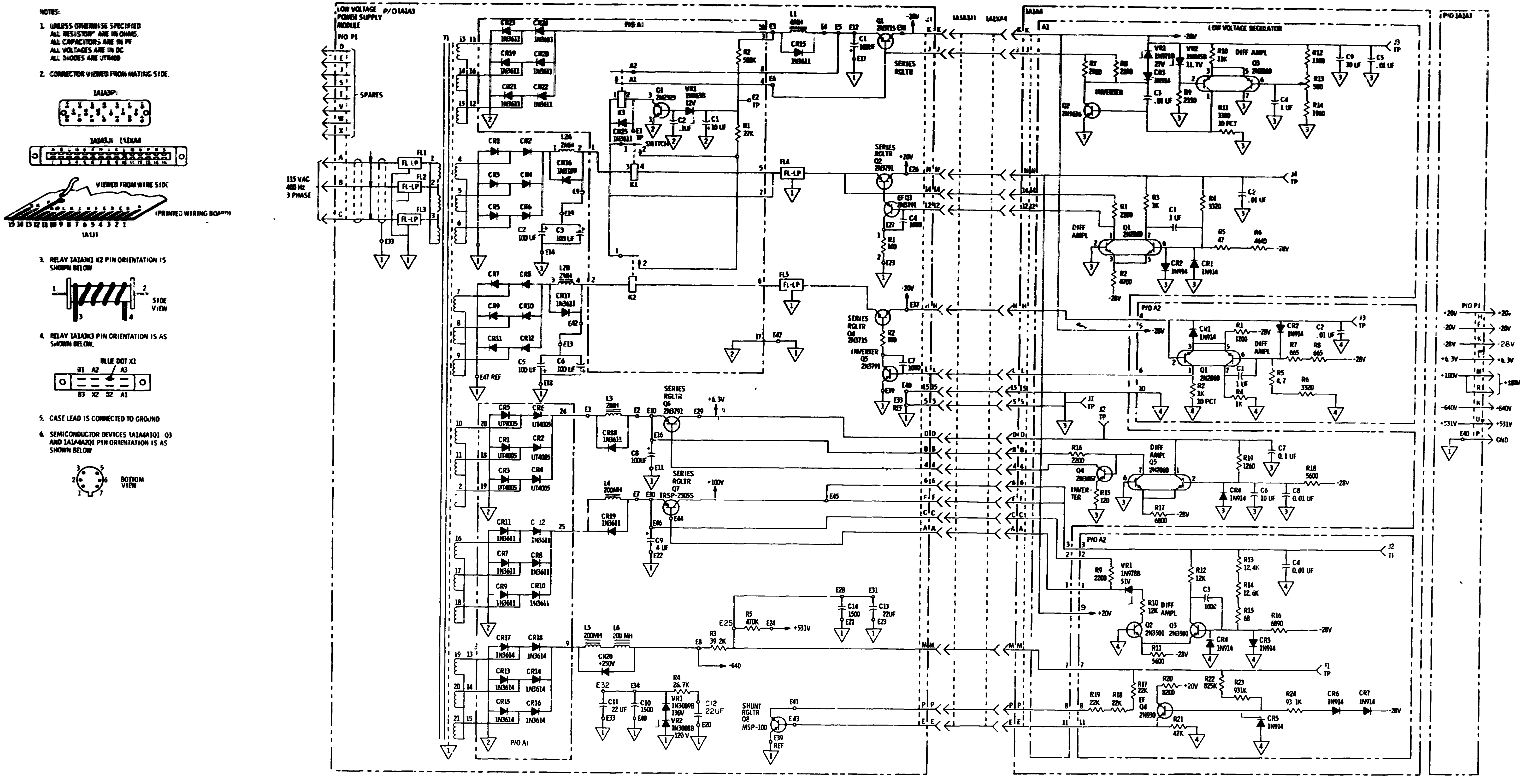


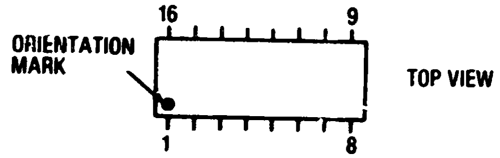
Figure FO-12. Low voltage power supply, 1A1A3, and regulator 1A1A4 schematic diagram

NOTES:

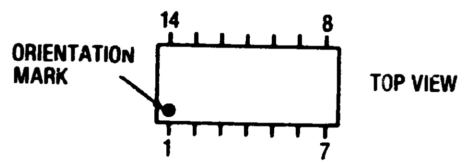
1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN FOR COMPLETE DESIGNATION PREFIX WITH 1A1A7
2. UNLESS OTHERWISE SPECIFIED:
   ALL RESISTORS ARE IN OHMS, ±5 PCT, 1/4 WATT.
   ALL CAPACITORS ARE IN UF
   ALL VOLTAGES ARE IN DC.
3. INTEGRATED CIRCUIT DEVICES U3 AND U4 ARE IDENTIFIED ON THE DRAWING BY THE UNDERLINED PORTION OF THE TYPE NUMBER LISTED BELOW. VOLTAGE AND GROUND PINS ARE INDICATED.

REF DES	TYPE NUMBER	+5V PIN	GND PIN
U3	SN54LS03	14	7
U4	SN54LS05	14	7

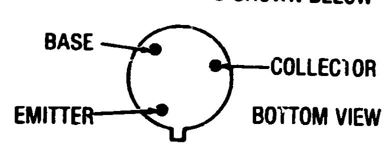
4. PIN ORIENTATION FOR INTEGRATED CIRCUIT DEVICE U2 IS SHOWN BELOW



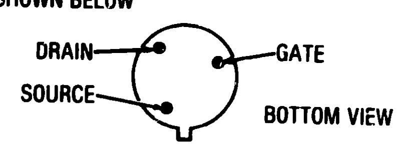
5. PIN ORIENTATION FOR INTEGRATED CIRCUIT DEVICES U3 AND U4 IS SHOWN BELOW



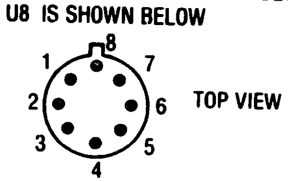
6. PIN ORIENTATION FOR SEMICONDUCTOR DEVICES Q1, Q2, Q4, AND Q5 THRU Q11 IS SHOWN BELOW

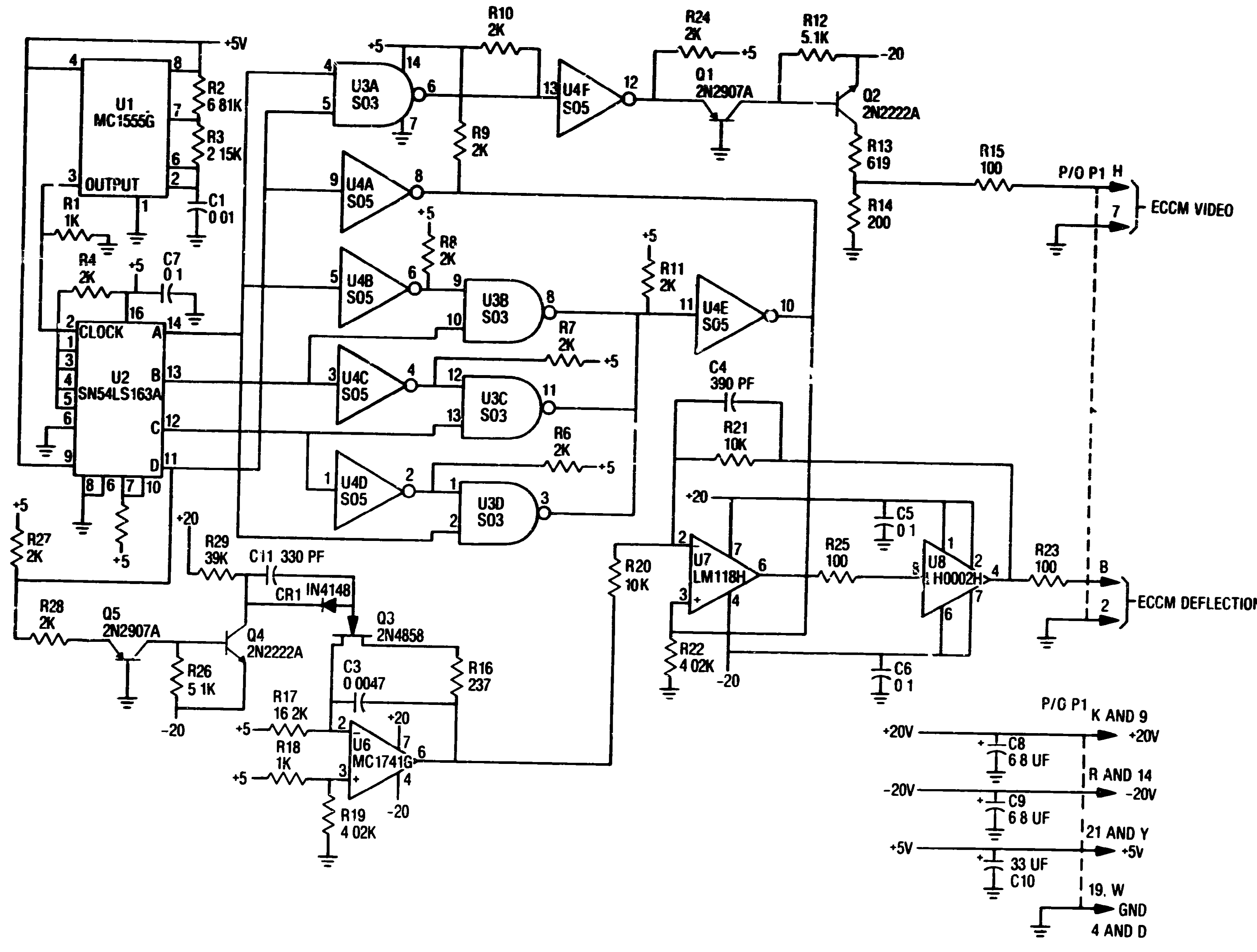


7. PIN ORIENTATION FOR SEMICONDUCTOR DEVICE Q3 IS SHOWN BELOW



8. PIN ORIENTATION FOR INTEGRATED CIRCUIT DEVICES U1, U6, U7, AND U8 IS SHOWN BELOW





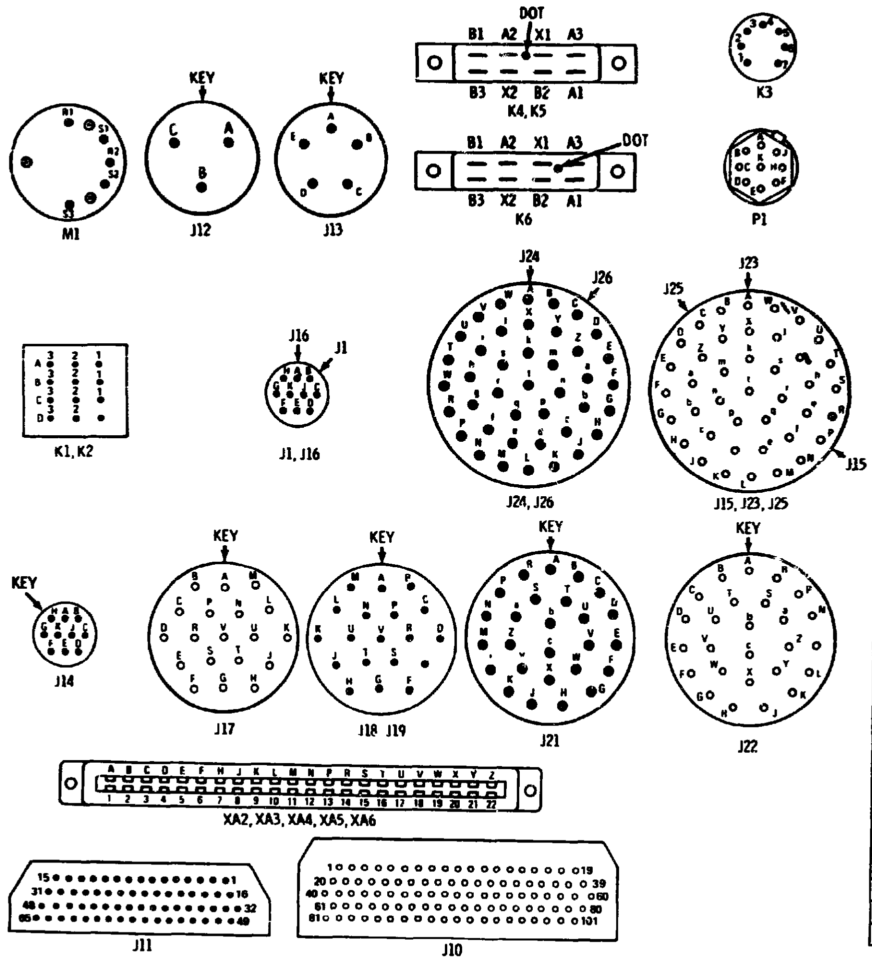
EL3AG074

Figure FO-13. Monitor- adapter input simulator, schematic diagram

NOTES.

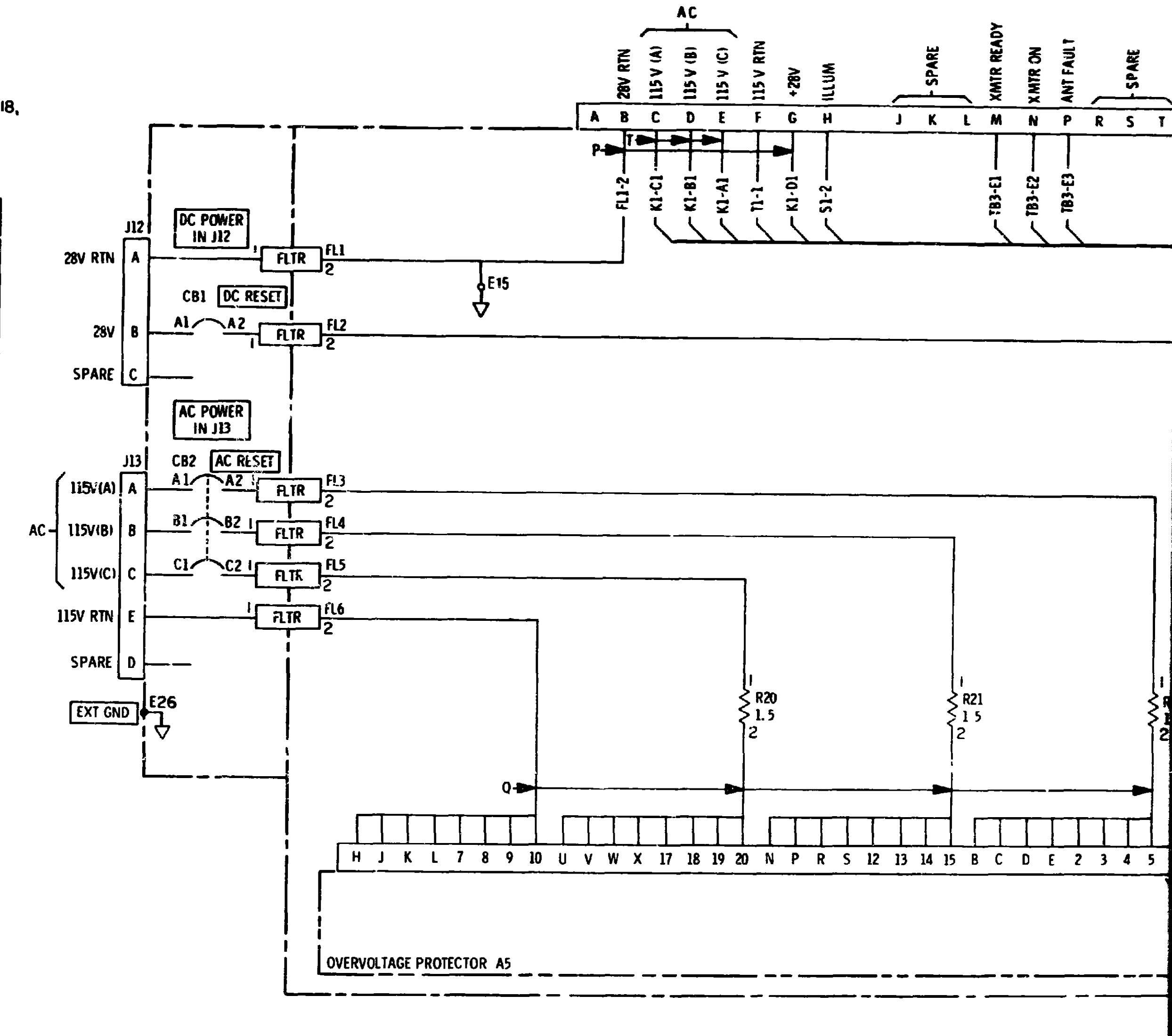
1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. FOR COMPLETE DESIGNATIONS PREFIX WITH 1A2.
2. UNLESS OTHERWISE SPECIFIED-
   ALL RESISTORS ... OHMS
   ALL VOLTAGE ... IN DC
3. ... MARKINGS.
4. PINS OF CONNECTORS J10 AND J11 ARE CONNECTED TO LIKE-NUMBERED TEST JACKS ON THE FRONT PANEL WITH THE EXCEPTIONS NOTED BELOW

CONN	PINS NOT CONNECTED TO TEST JACKS
J10	52, 68, 84, 89, 90, 91, 92, 94, 95, 100
J11	6, 12, 19, 20, 25, 26, 31, 34, 48, 53, 56, 60, 62, 63



PINS OF CONNECTORS J1, J14, J15, J16, J18, J20, J22, J24 AND J26 ARE CONNECTED TO TEST JACKS ON THE FRONT PANEL IN ACCORDANCE WITH THE TABLES BELOW. EXCEPTIONS ARE BLANK.

PINS	J15	J16	J18	J20	J22	J24	J26
A	1	1	1	1	1	1	1
B	2	2	2	2	2	2	2
C	3	3	3	3	3	3	3
D			4	4	4	4	4
E		5	5	5	5	5	5
F	6		6	6	6	6	6
G		7	7		7	7	7
H		8	8		8	8	8
J			9		9	9	9
K		10	10			10	10
L	11			11		11	11
M	12			12	12	12	12
N	13		13	13	13	13	13
P	14		14	14	14	14	
R	15		15	15	15	15	15
S	16		16	16	16	16	16
T	17		17	17	17	17	
U	18		18	18	18	18	
V	19		19	19	19	19	19
W	20				20	20	
X	21				21		21
Y	22				22		22
Z	23				23		23
a	24				24	24	24
b					25	25	25
c	26				26	26	26
d							27
e						28	28
f						29	29
g						30	30
h						31	31
i						32	32
j						33	33
k							34
m						35	35
n						36	36
p						37	37
q						38	38
r						39	39
s							40
t						41	41



PINS	A	B	C	D	E	F	G	H	J	K
J1	1	2	3	4	5	6	7	8	9	10
J14			3	4		6		8	9	10

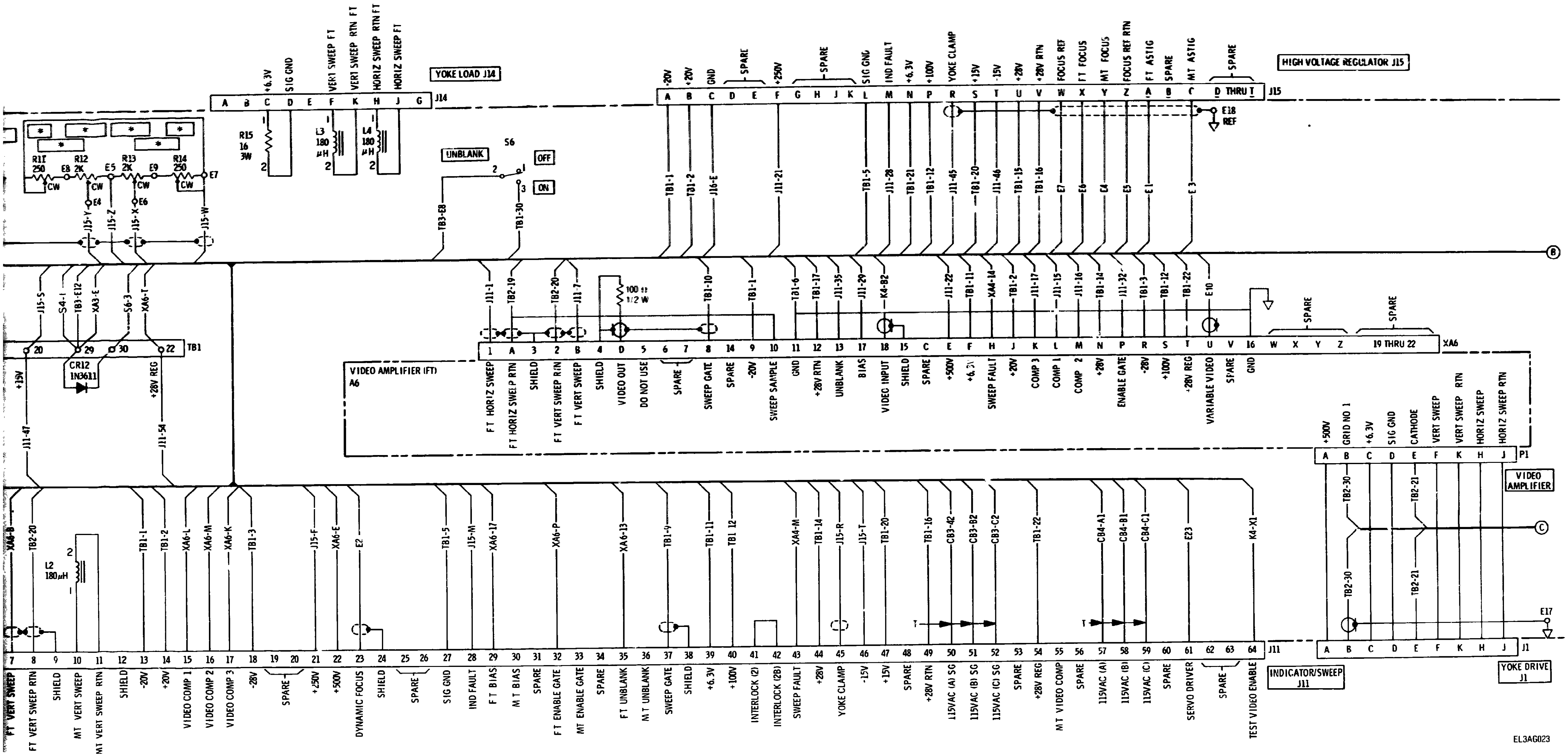


Figure FO-14. Test Set Subassembly MX-8638A/APS-94D, Unit 1A2, interconnection diagram (sheet 2 of 4)

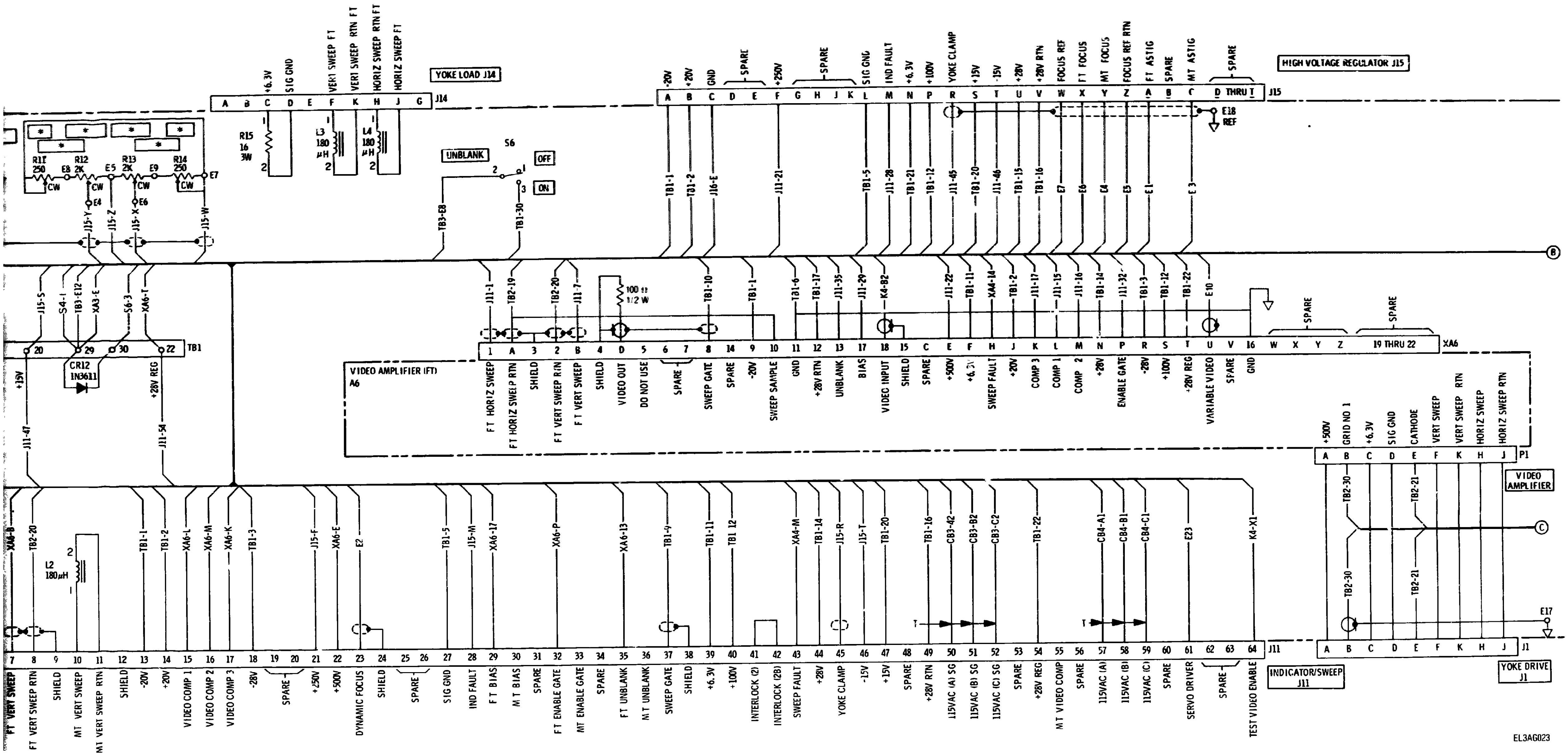


Figure FO-14. Test Set Subassembly MX-8638A/APS-94D, Unit 1A2, interconnection diagram (sheet 2 of 4)

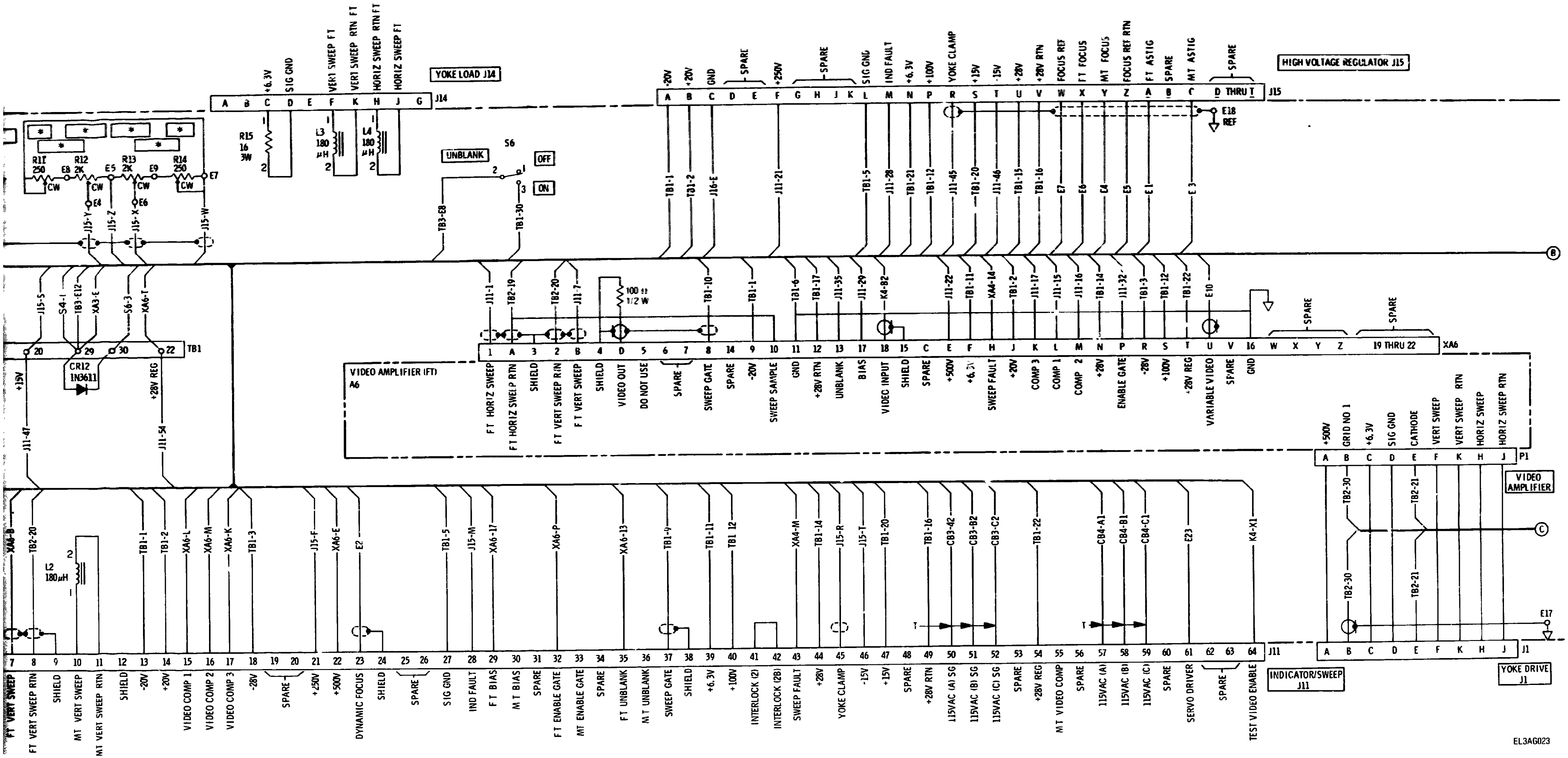
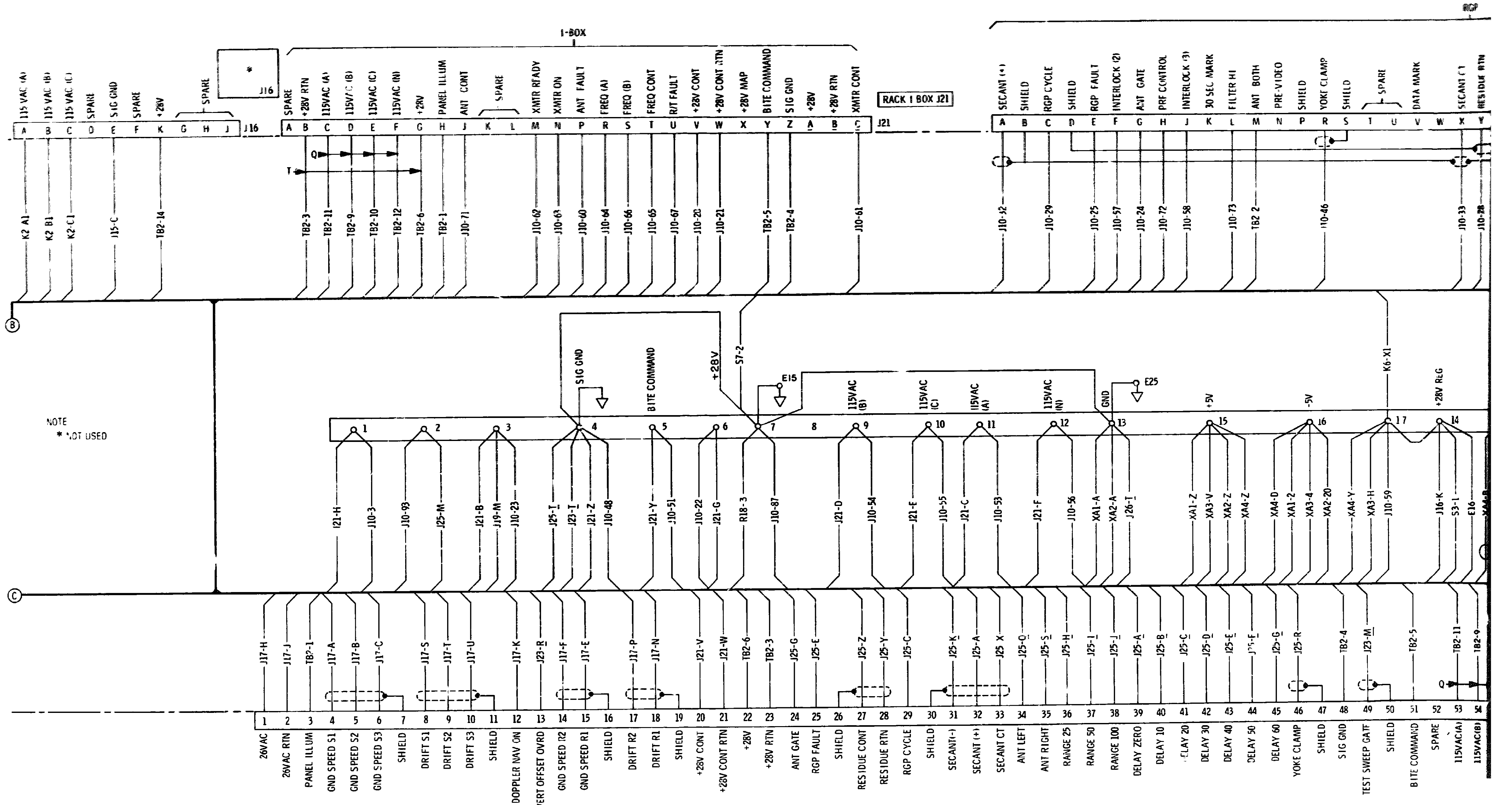


Figure FO-14. Test Set Subassembly MX-8638A/APS-94D, Unit 1A2, Interconnection diagram (sheet 2 of 4)



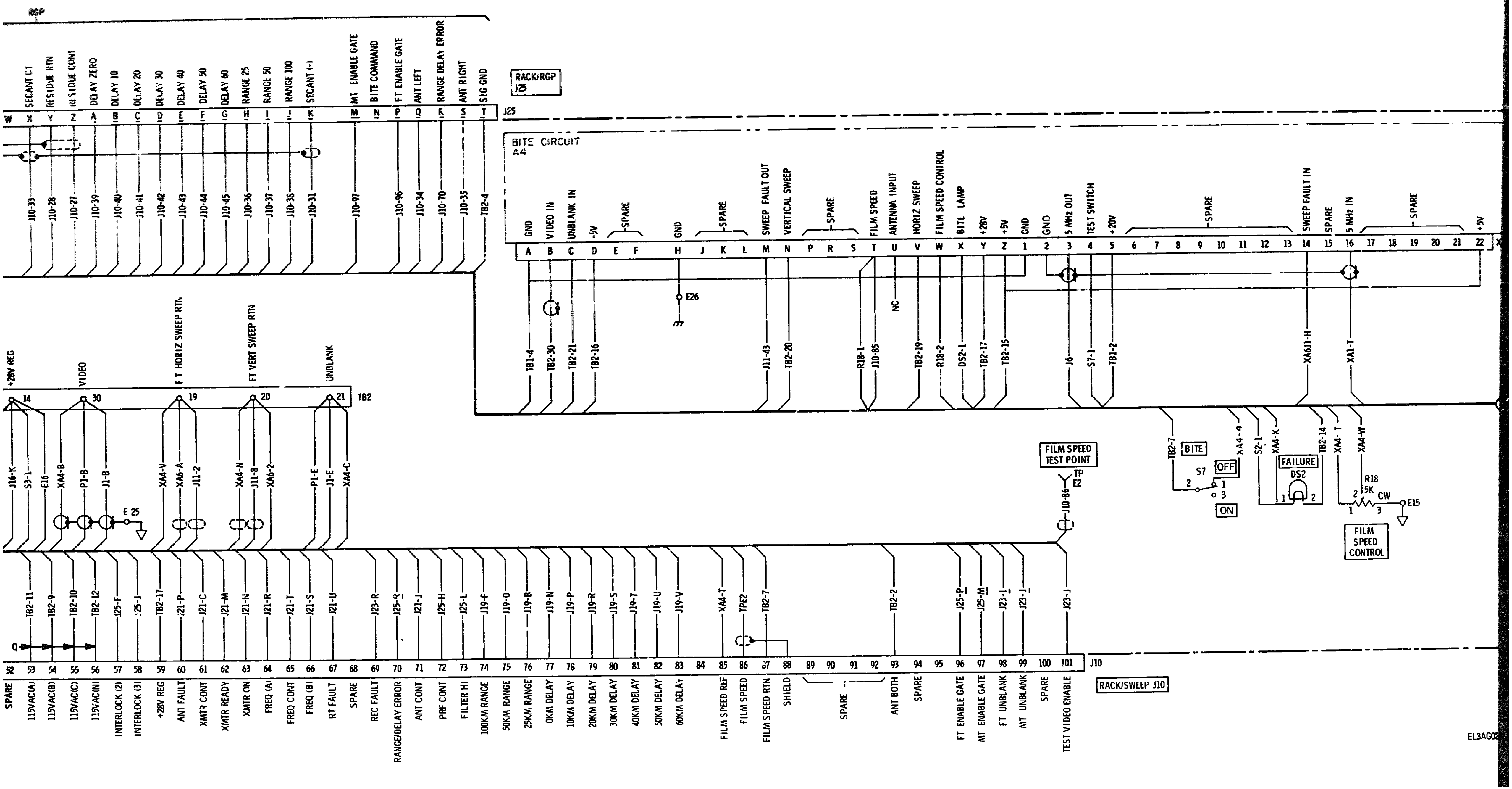


Figure FO-14. Test Set Subassembly MX-8638A/APS-94D, Unit 1A2, interconnection diagram (sheet 3 of 4)

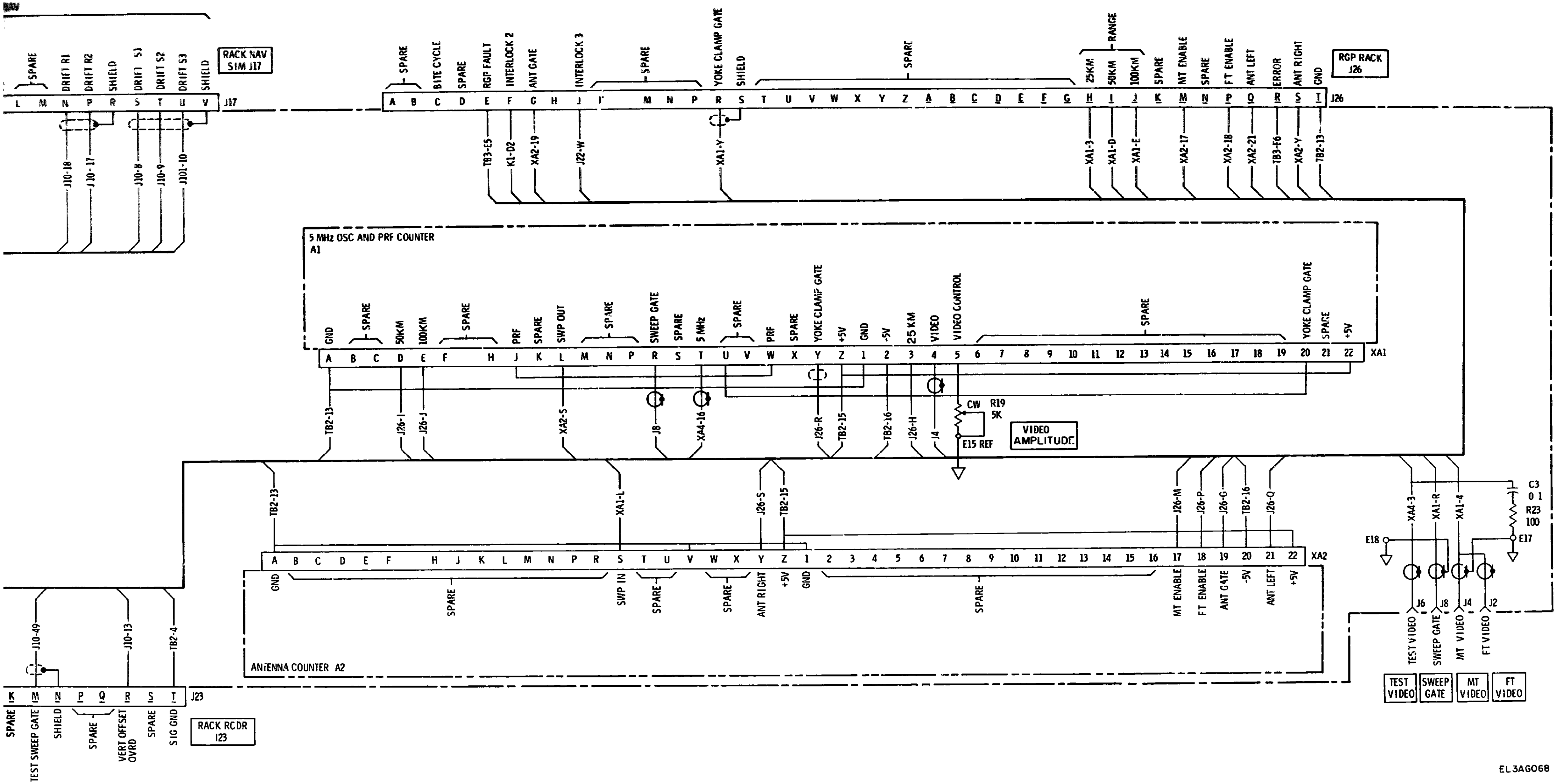


Figure FO-14. Test Set Subassembly MX-8638A/APS-94D. Unit 1A2, interconnection diagram (sheet 4 *of 4)*

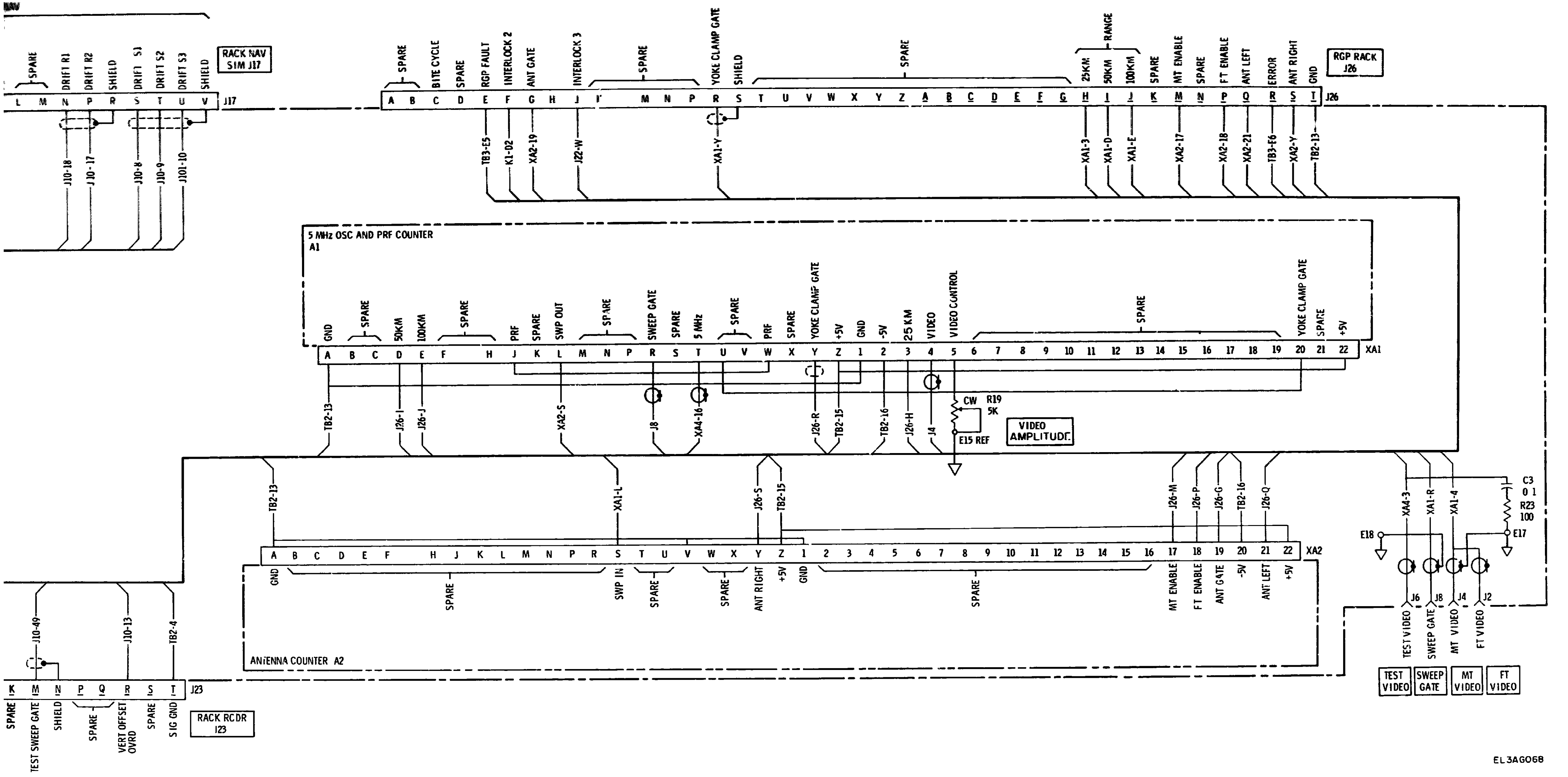


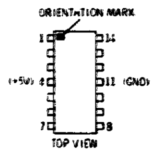
Figure FO-14. Test Set Subassembly MX-8638A/APS-94D. Unit lA2, interconnection diagram (sheet 4 of 4)

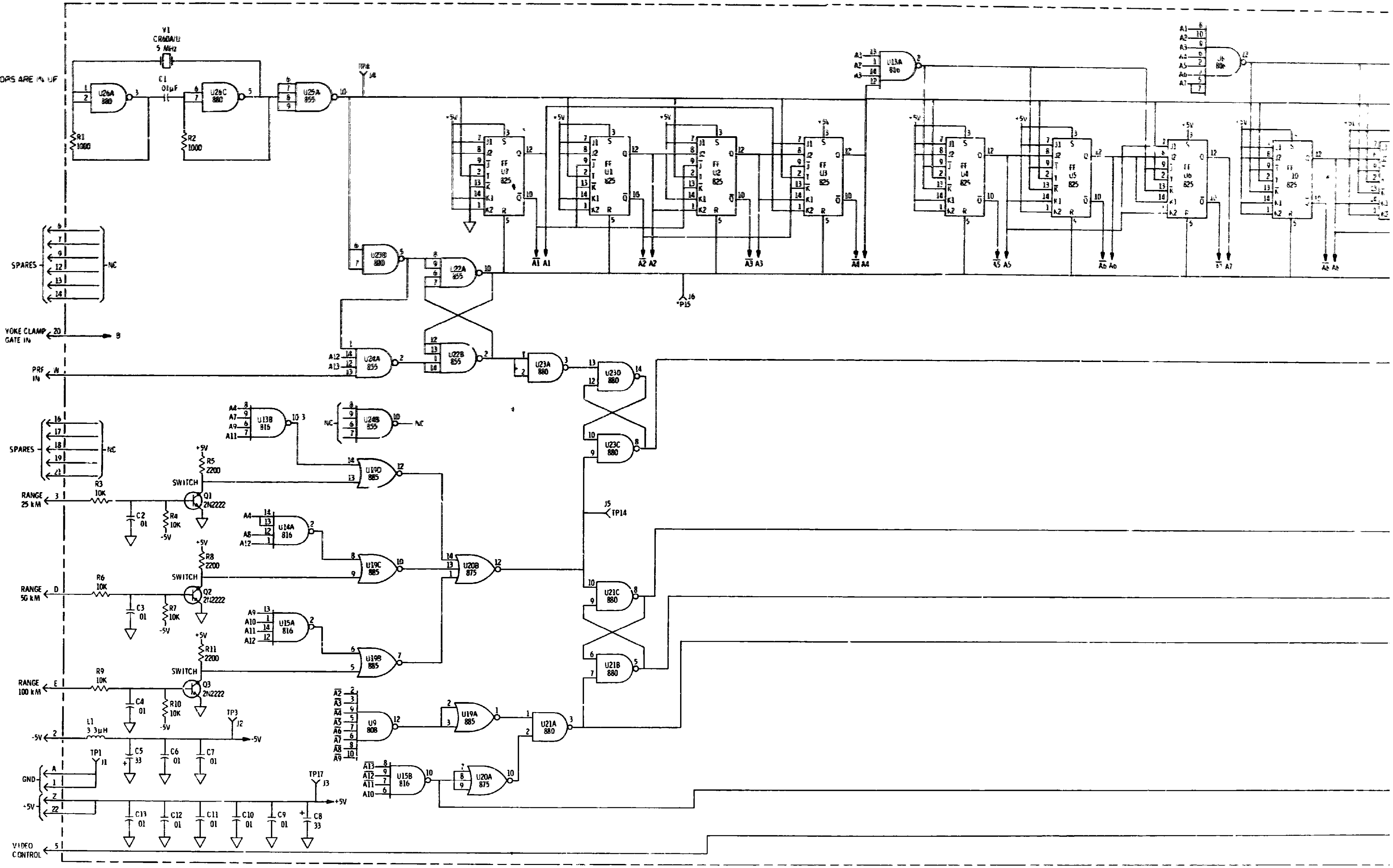
NOTES:

1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. FOR COMPLETE DESIGNATIONS PREFIX WITH 1A2A1

2. UNLESS OTHERWISE SPECIFIED
   ALL RESISTORS ARE IN OHMS, ALL CAPACITORS ARE IN UF
   ALL DIODES ARE 1N914.

3. INTEGRATED CIRCUIT DEVICES U1 THRU U26 HAVE PARTIAL TYPE NUMBERS SHOWN. FOR COMPLETE TYPE NUMBER PREFIX WITH S8 AND SUFFIX WITH J
   EXAMPLE. 880 - SHOWN
   S8880J - TYPE NO
   PIN ORIENTATION IS AS SHOWN BELOW





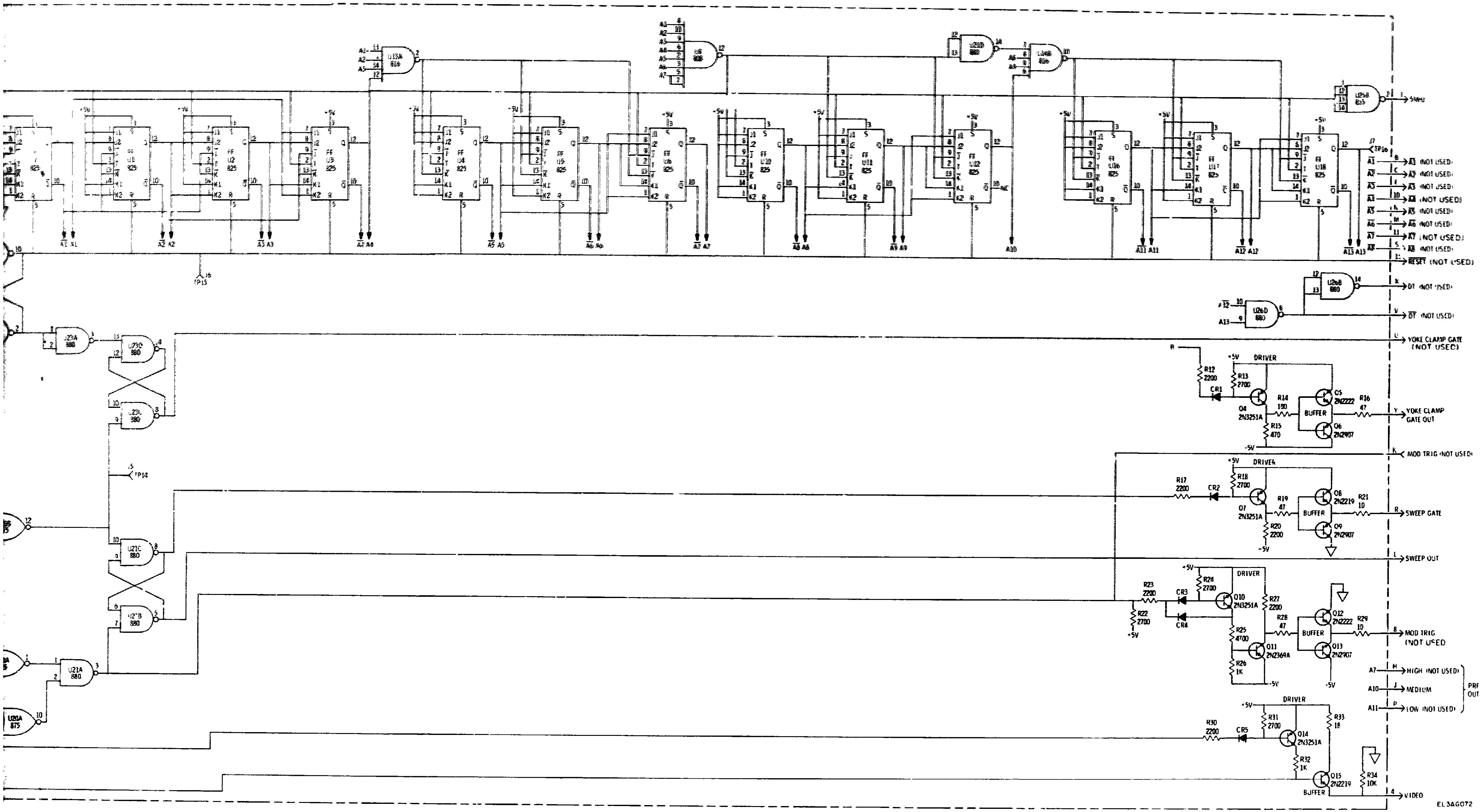


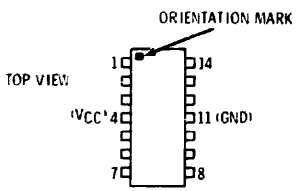
Figure FO-15. Five-MHz oscillator and prf counter, 1A2A1, schematic diagram

NOTES

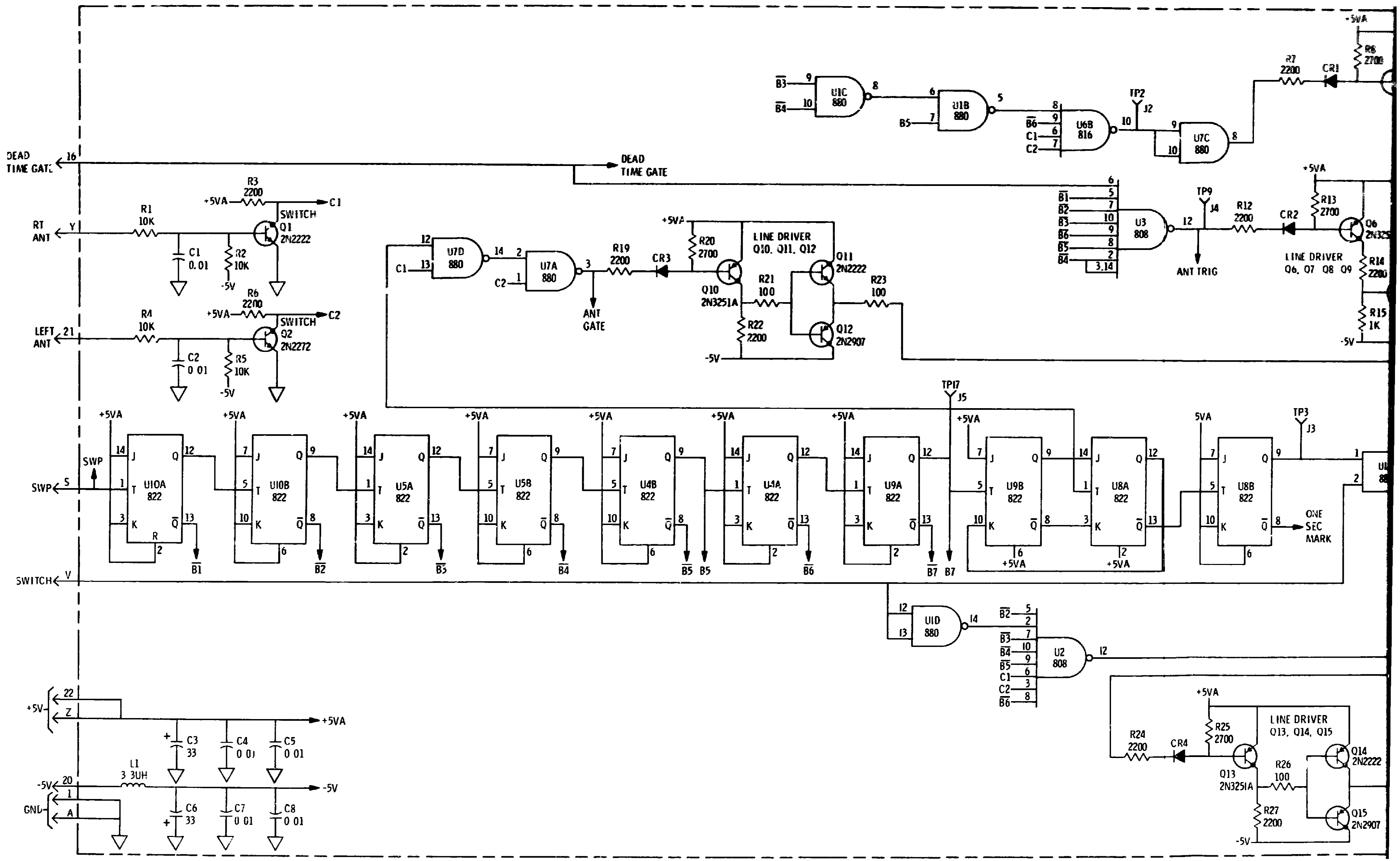
1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN FOR COMPLETE DESIGNATIONS PREFIX WITH 1A2A2.

2. UNLESS OTHERWISE SPECIFIED ALL
ALL RESISTORS ARE IN OHMS
ALL CAPACITORS ARE IN µF
ALL DIODES ARE 1N914

3. INTEGRATED CIRCUIT DEVICES U1 THRU U23 HAVE PARTIAL TYPE NUMBERS SHOWN FOR COMPLETE TYPE NUMBER PREFIX WITH S8 AND SUFFIX WITH J
EXAMPLE 880 SHOWN
S8880J - TYPE NO
PIN ORIENTATION IS AS SHOWN BELOW



U1 THRU U10 ARE +5V A AT (V_{CC}) PIN 4.
U11 THRU U23 ARE +5V B AT (V_{CC}) PIN 4.



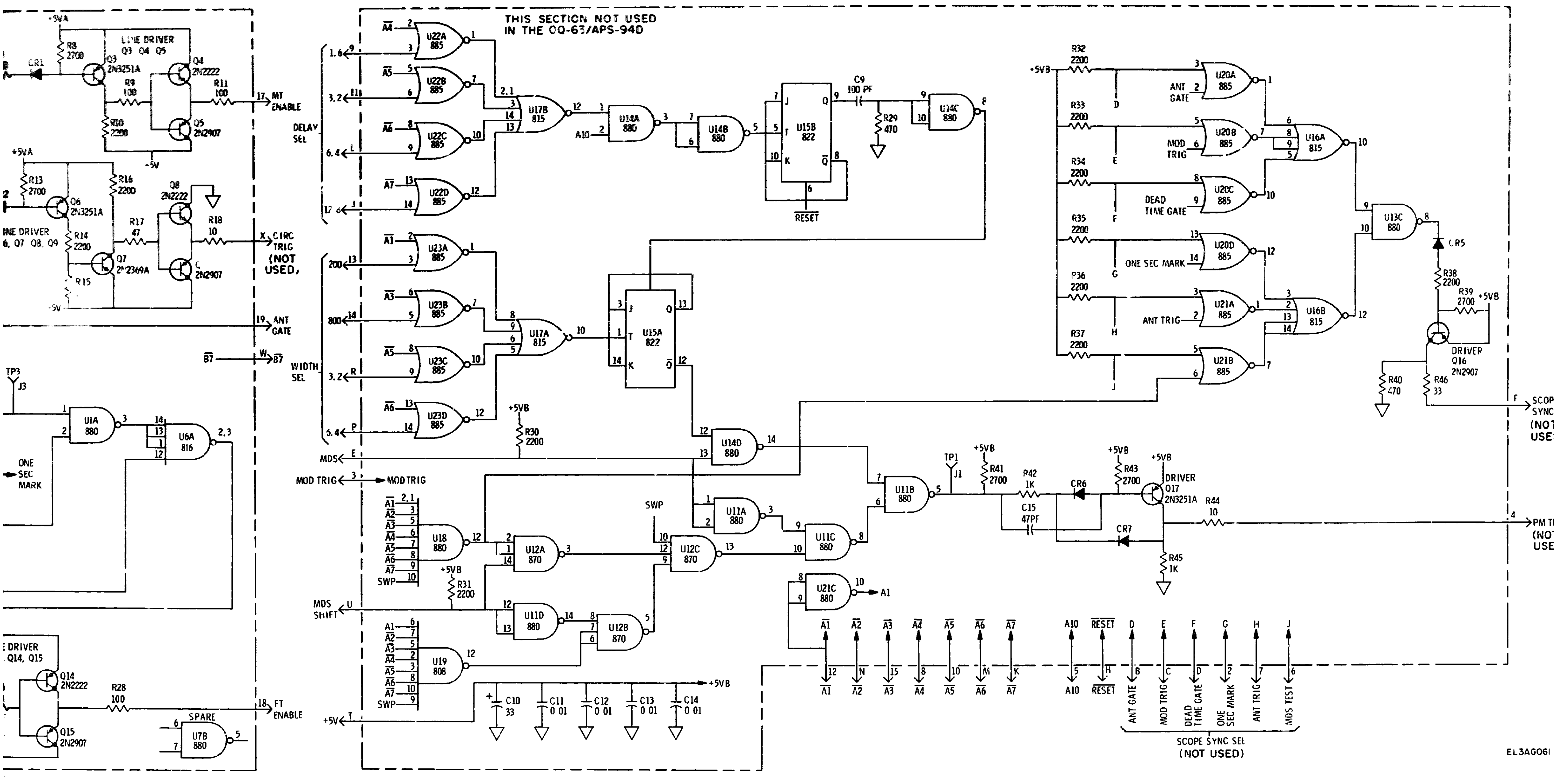


Figure FO-16. Antenna counter, 1A2A2, schematic diagram

NOTES

1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. FOR COMPLETE DESIGNATIONS PREFIX WITH 1A2A3
2. UNLESS OTHERWISE SPECIFIED ALL RESISTORS ARE IN OHMS. ALL CAPACITORS ARE IN pF.
3. TERMINATIONS CODED WITH THE SAME LETTERS ARE ELECTRICALLY CONNECTED.

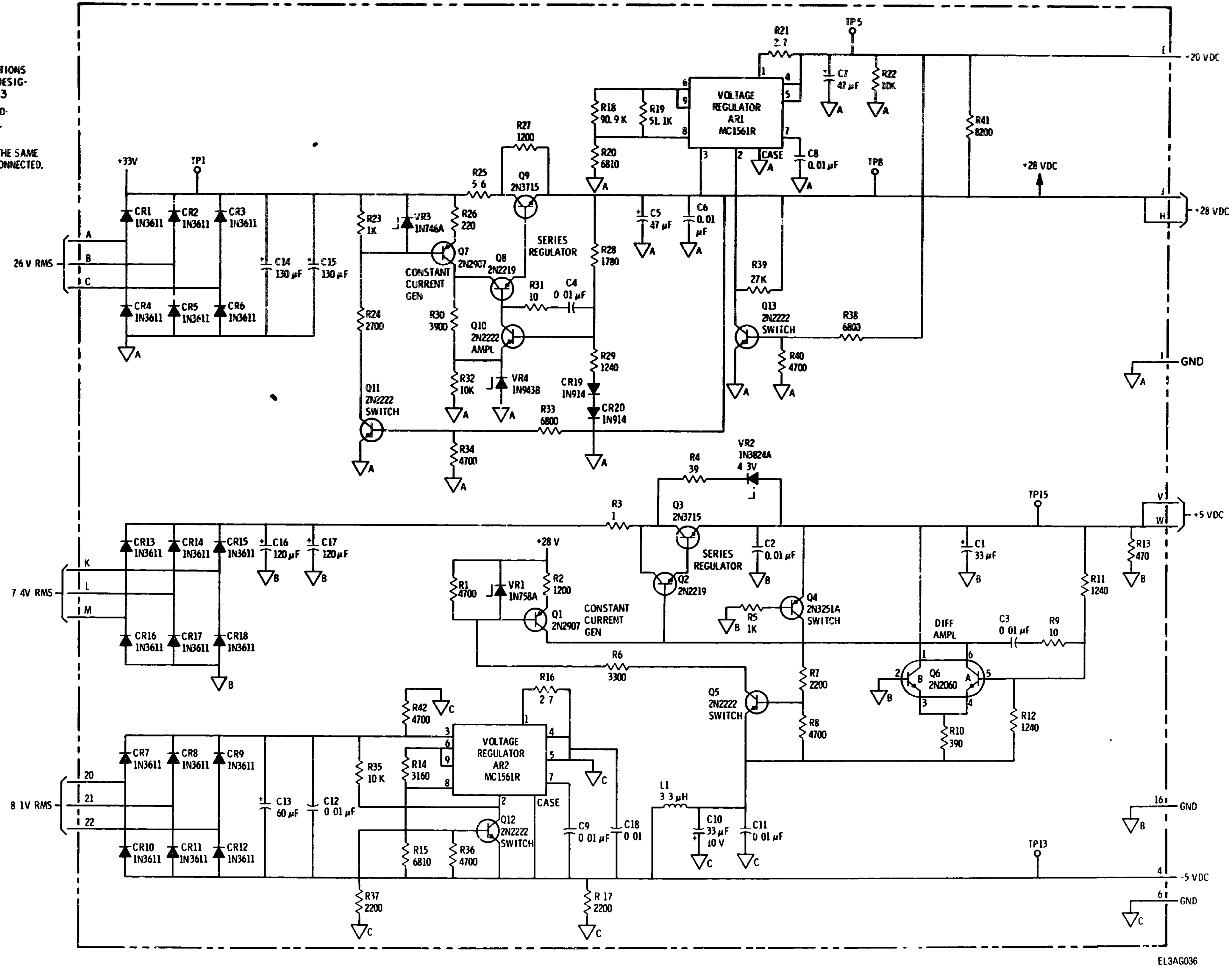


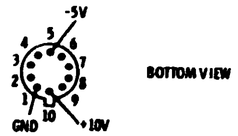
Figure FO-17. Low voltage power supply regulator, 1A2A3, schematic diagram

NOTES:

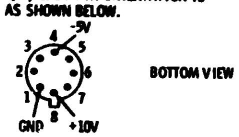
1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. FOR COMPLETE DESIGNATIONS PREFIX WITH 1A2A4.

2. UNLESS OTHERWISE SPECIFIED
   ALL RESISTORS ARE IN Ω
   ALL CAPACITORS μF
   ALL DIODES ARE 1N914

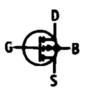
3. INTEGRATED CIRCUIT DEVICES AR2, 4, 6, and 8 PIN ORIENTATION IS AS SHOWN BELOW



4. INTEGRATED CIRCUIT DEVICES AR1, 3, 5, and 7 PIN ORIENTATION IS AS SHOWN BELOW.



5. SEMICONDUCTOR DEVICES Q2 AND Q3 PIN ORIENTATION IS AS SHOWN BELOW.



SYMBOL INDICATES P CHANNEL MOS-16FET DESIGNED FOR ENHANCEMENT MODE OPERATION.

6. L3 AND L4 ARE FERRITE BEADS, FERROXCUBE PART NO 56-590-65/3B

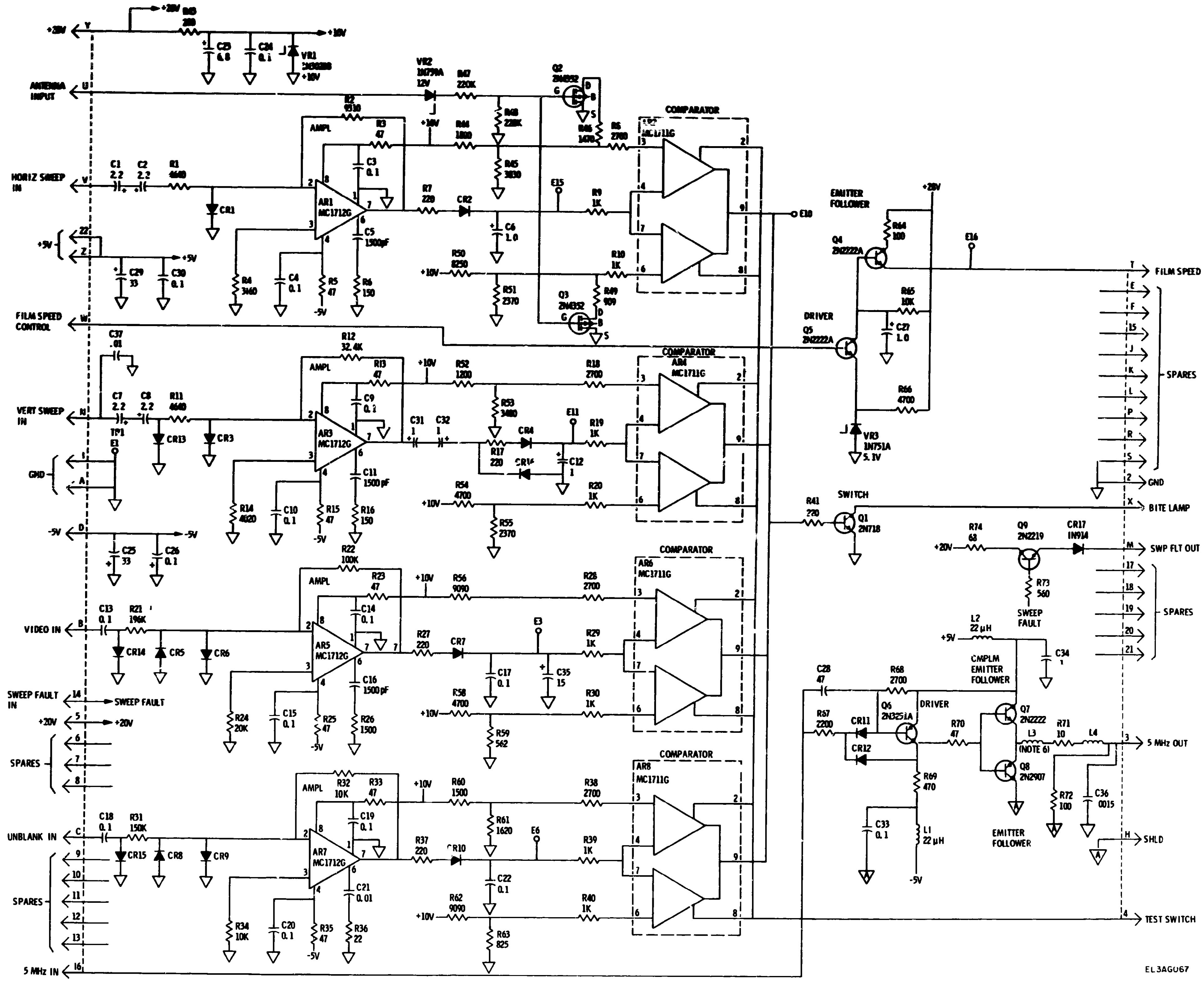


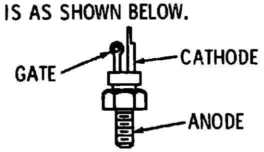
Figure FO-18. BITE circuit, 1A2A4, schematic diagram

NOTES:

1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. FOR COMPLETE DESIGNATIONS PREFIX WITH 1A2A5.

2. UNLESS OTHERWISE SPECIFIED
   ALL RESISTORS ARE IN OHMS.
   ALL CAPACITORS ARE IN μF.
   ALL DIODES ARE 1N3612.

3. PIN ORIENTATION OF SCR Q2, Q5, Q7, Q10, Q12, AND Q15 IS AS SHOWN BELOW.



4. SYMBOL MEANS SCR.

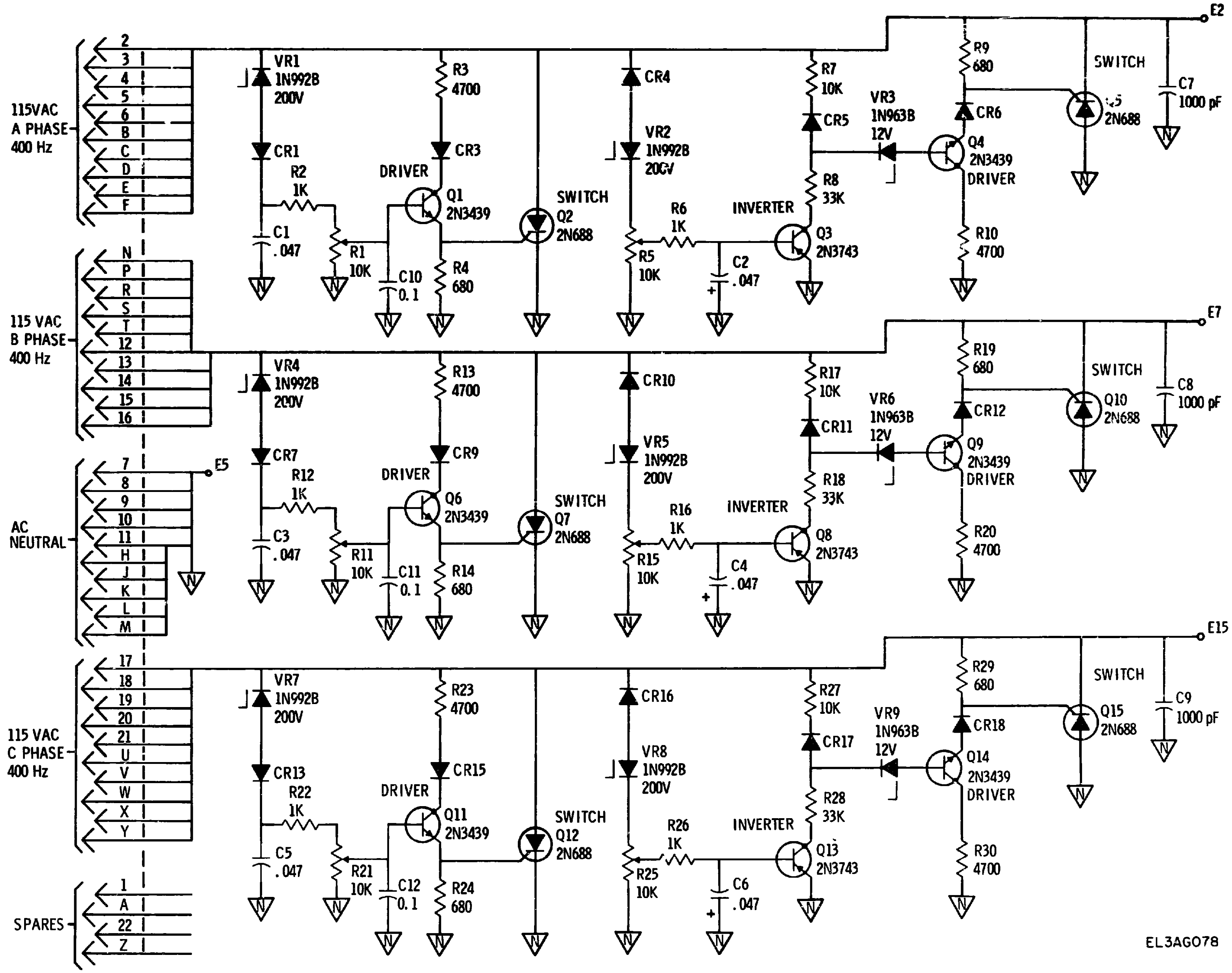


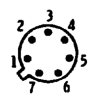
Figure FO-19. *Overvoltage* protection circuit, *1A2A5*, schematic diagram

NOTES

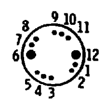
1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. FOR COMPLETE DESIGNATIONS PREFIX WITH 1A2A6.

2. UNLESS OTHERWISE SPECIFIED
ALL RESISTORS ARE IN OHMS.
ALL CAPACITORS ARE IN µF.
ALL INDUCTORS ARE IN µH.
ALL DIODES ARE 1N914.

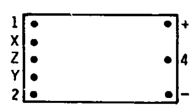
3. SEMICONDUCTOR DEVICE A1Q9 PIN ORIENTATION IS AS SHOWN BELOW.



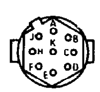
4. HEATER DEVICES A2HR1, AND 3, PIN ORIENTATION IS AS SHOWN BELOW.

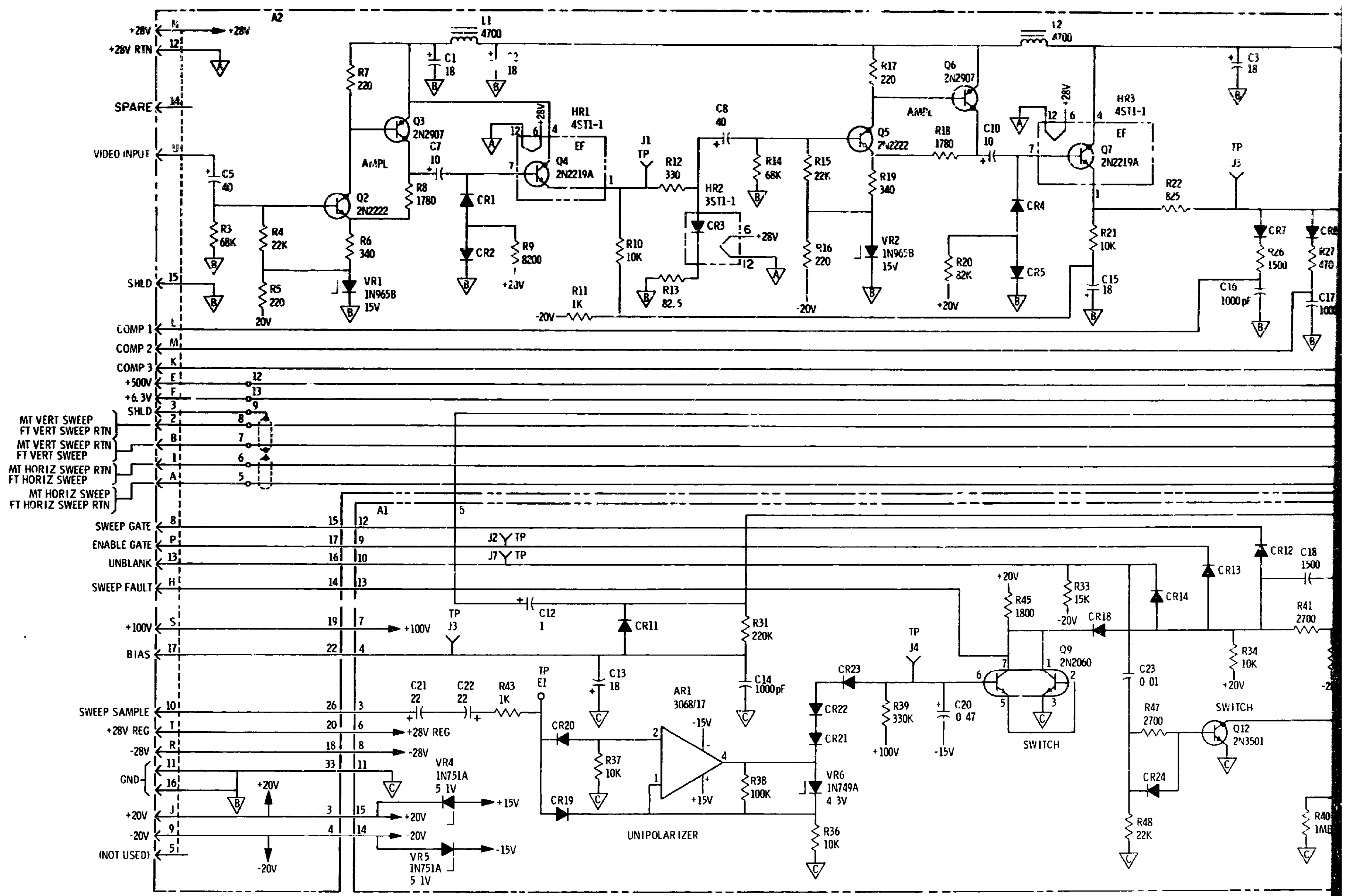


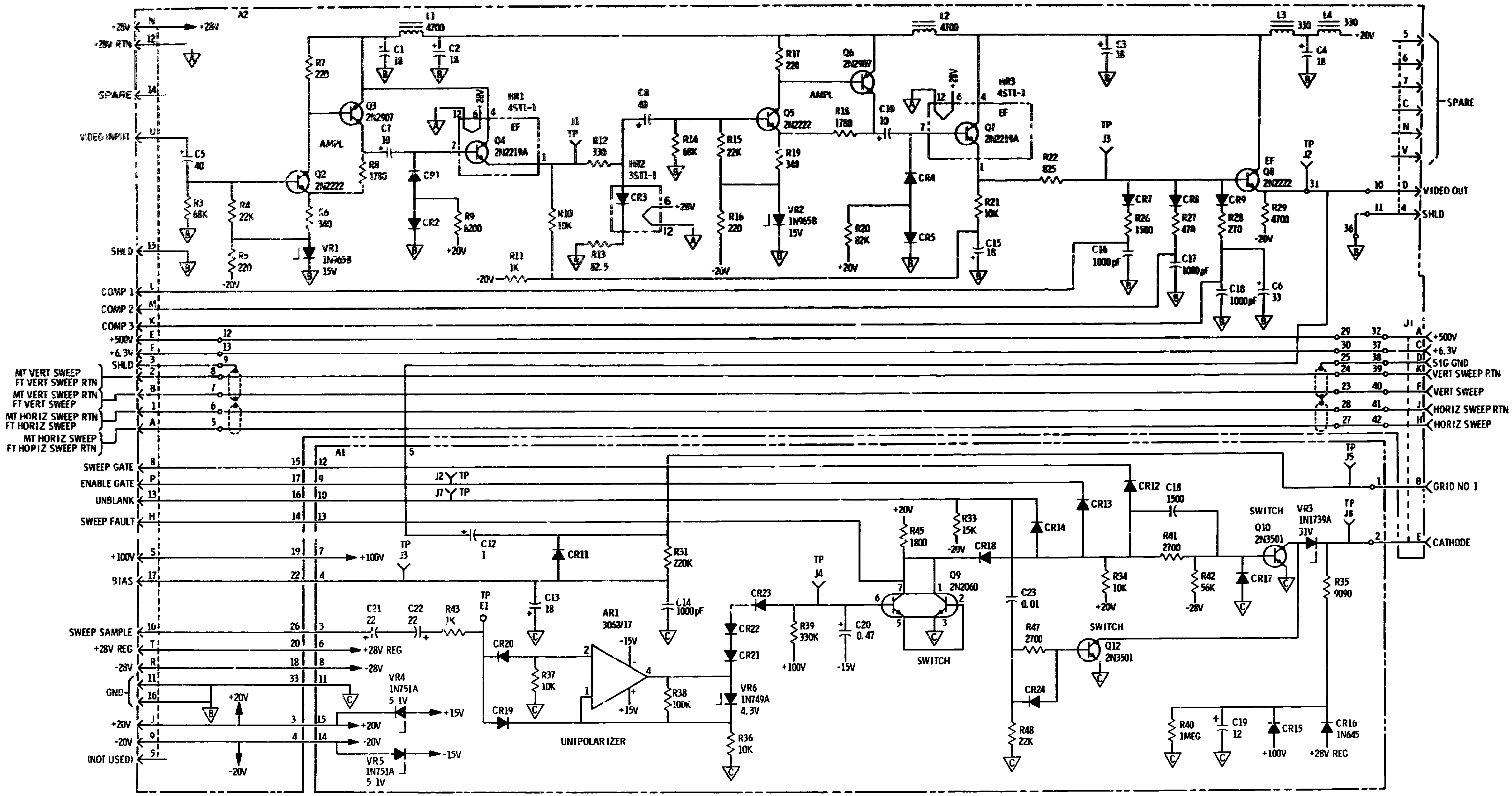
5. INTEGRATED CIRCUIT DEVICE A1AR1 PIN ORIENTATION IS AS SHOWN BELOW



6. CONNECTOR VIEWED FROM MATING SIDE







EL3AG030

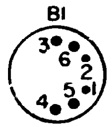
Figure FO-20. Video amplifier, 1A2A6, schematic diagram

NOTES:

1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. FOR COMPLETE DESIGNATIONS PREFIX WITH 2.

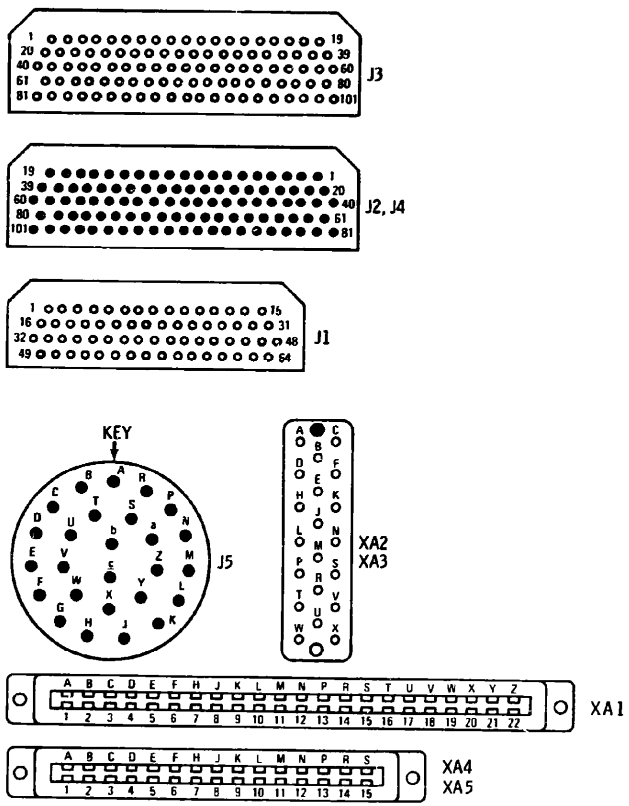
2. UNLESS OTHERWISE SPECIFIED: ALL RESISTORS ARE IN OHMS ALL VOLTAGES ARE IN DC.

3. MOTOR B1 PIN ORIENTATION IS AS SHOWN BELOW.



BOTTOM VIEWS

4. CONNECTORS VIEWED FROM MATING SIDE.

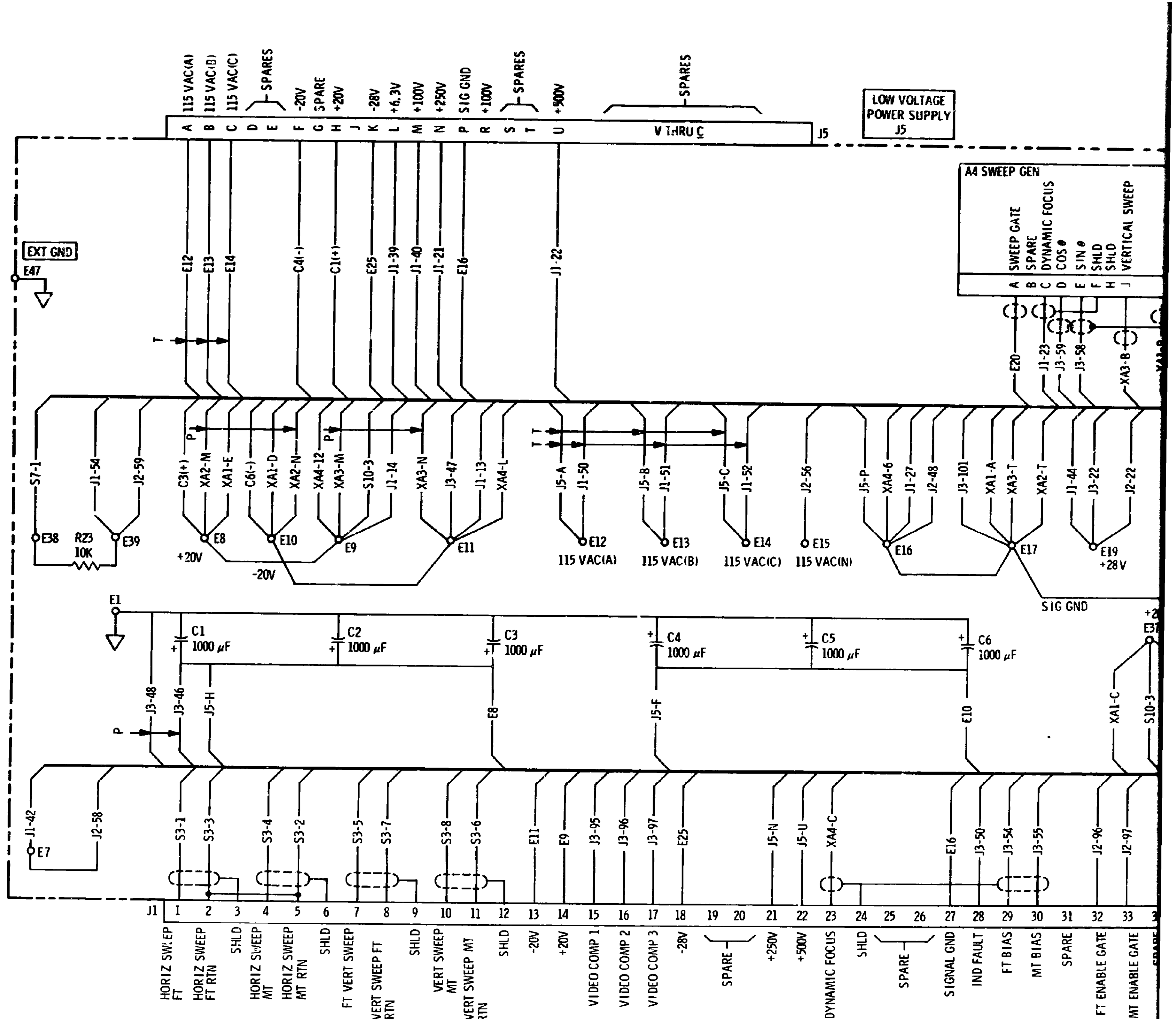


5. EACH PIN OF CONNECTOR J5 IS CONNECTED TO NUMBERED TEST JACKS ON THE FRONT PANEL IN ACCORDANCE WITH THE TABLE BELOW WITH THE EXCEPTIONS BLANKED OUT

A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	S	T	U	V	W	X	Y	Z	a	b	c	J5
1	2	3			6		8		10	11	12	13	14	15	16		18									TP

6. EACH PIN OF CONNECTORS J1, J2, J3, AND J4 ARE CONNECTED TO LIKE-NUMBERED TEST JACKS ON THE FRONT PANEL WITH THE EXCEPTIONS LISTED BELOW.

CONN	PINS NOT CONNECTED TO TEST JACKS
J1	19, 20, 25, 26, 31, 34, 48, 53, 56, 60, 62, 63
J2	52, 68, 84, 89, 90, 91, 92, 95, 100
J3	89, 90, 91, 92, 98, 99, 100
J4	89, 90, 91, 92, 94, 98, 99, 100



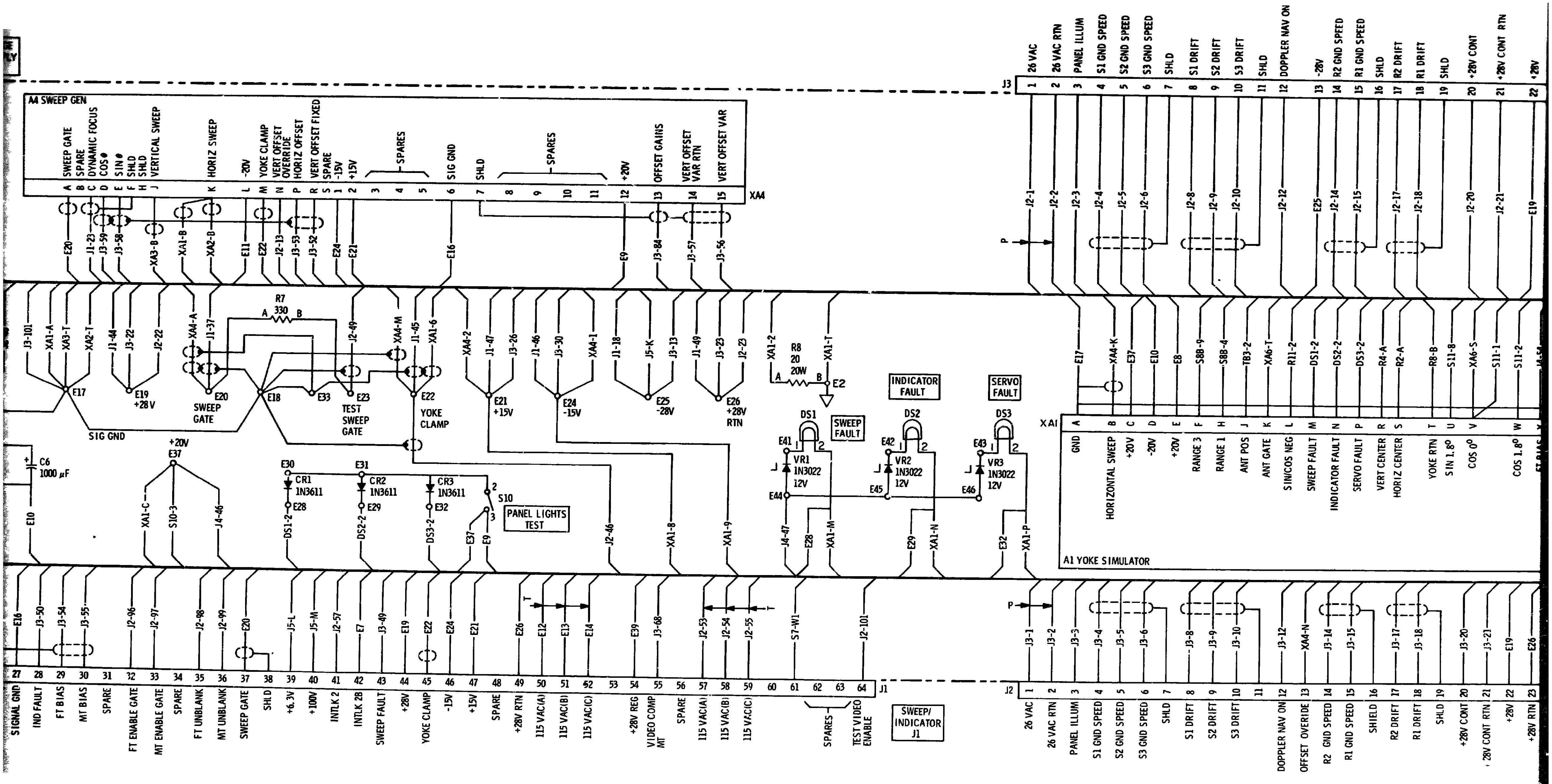


Figure FO-21. Test Set Subassembly MX-86

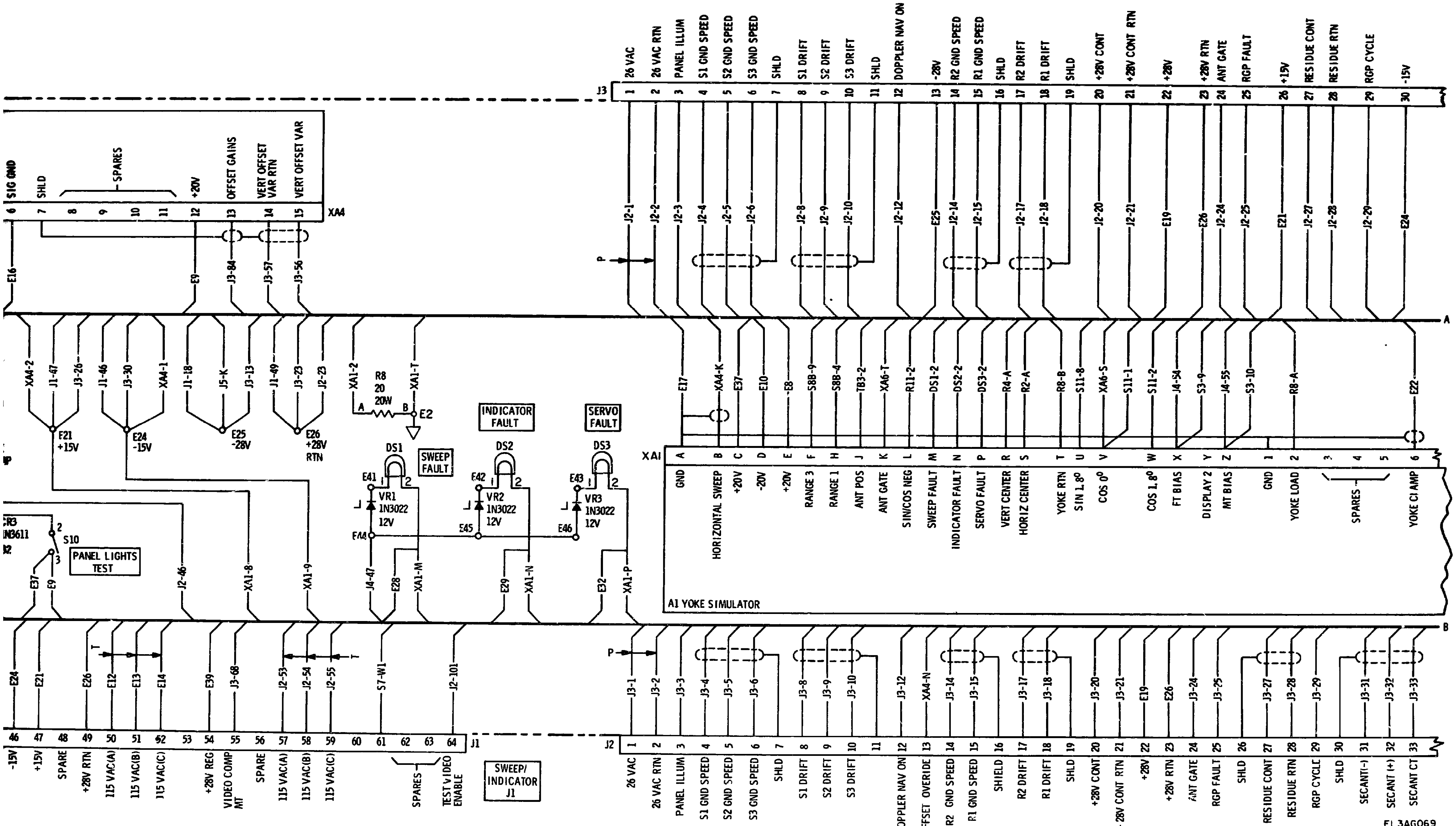


Figure FO-21 . Test Set Subassembly MX-8639A/APS-94-D, Unit 2 interconnection diagram (sheet 1 of 4)

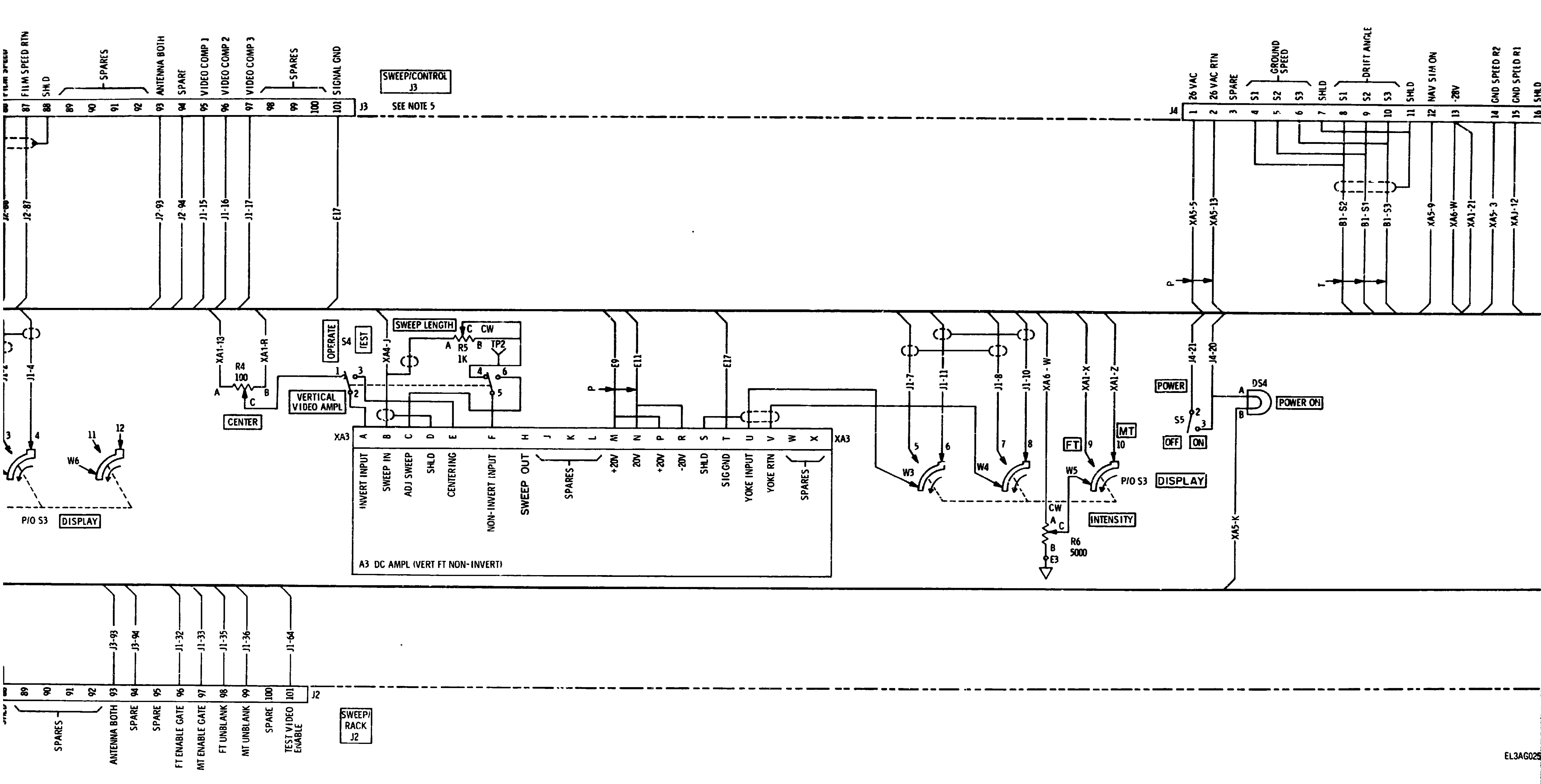


Figure FO-21. Test Set Subassembly MX-8639A/APS-94D, Unit 2 interconnection diagram (sheet 2 of 4)

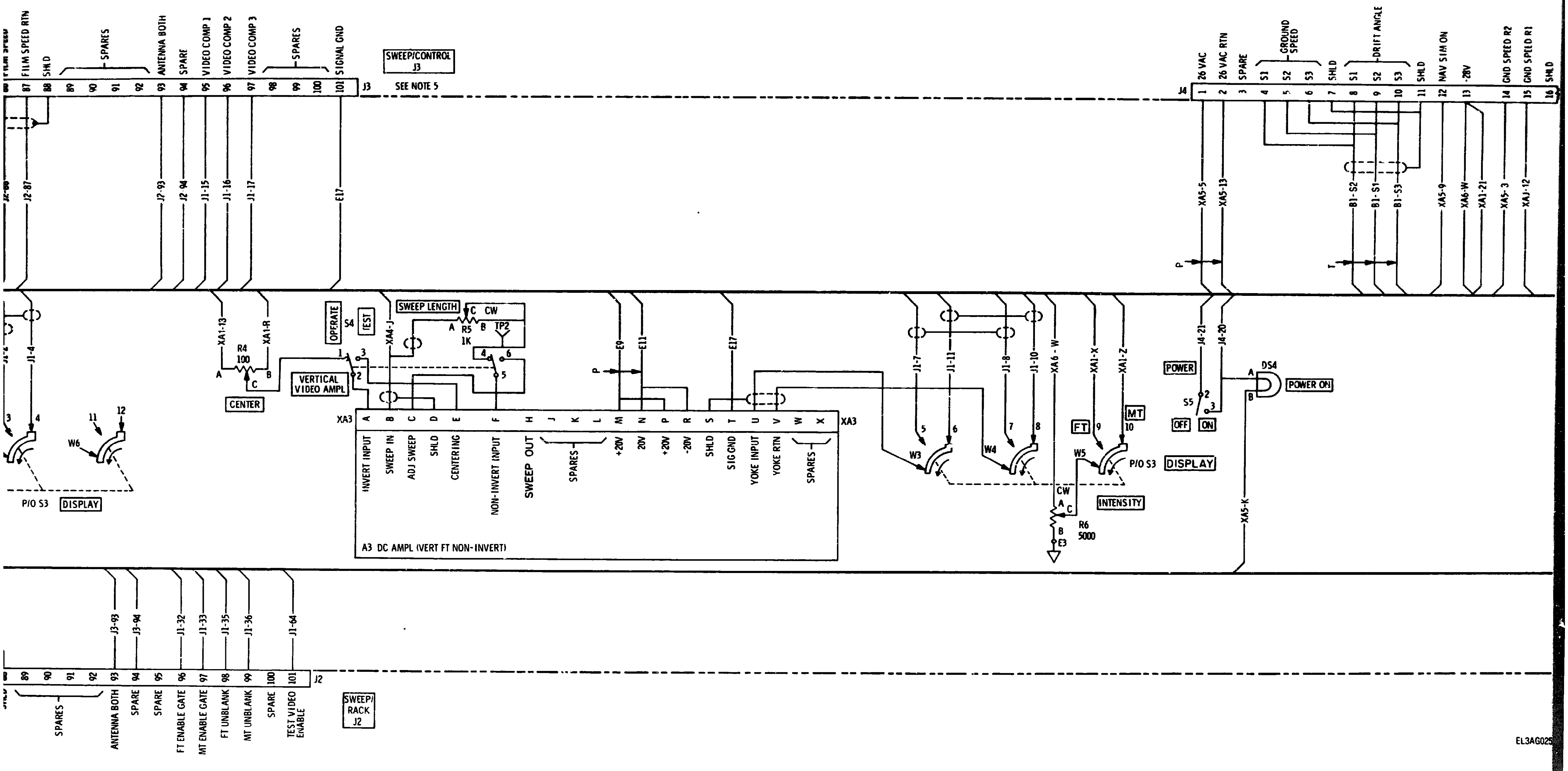
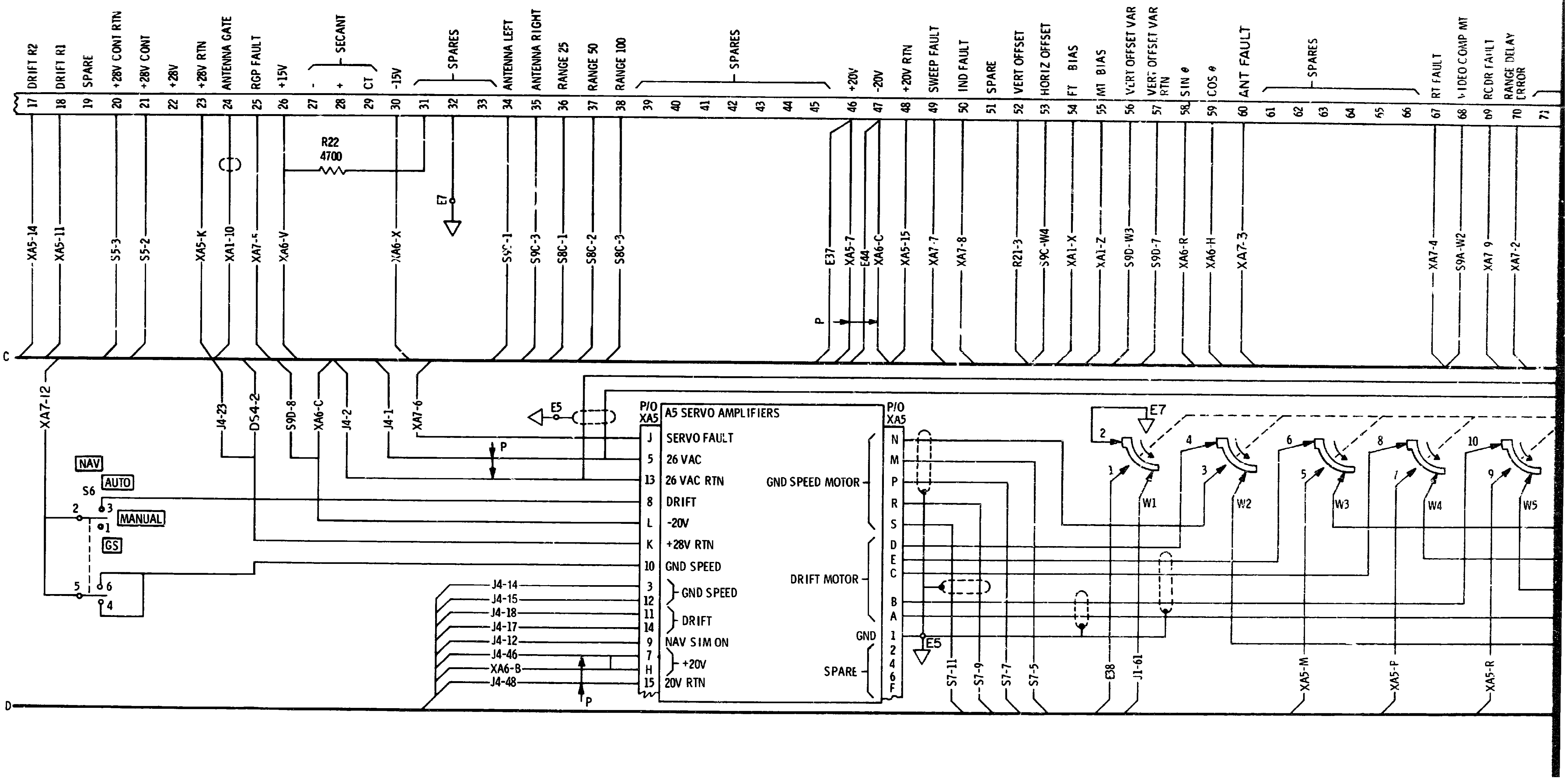
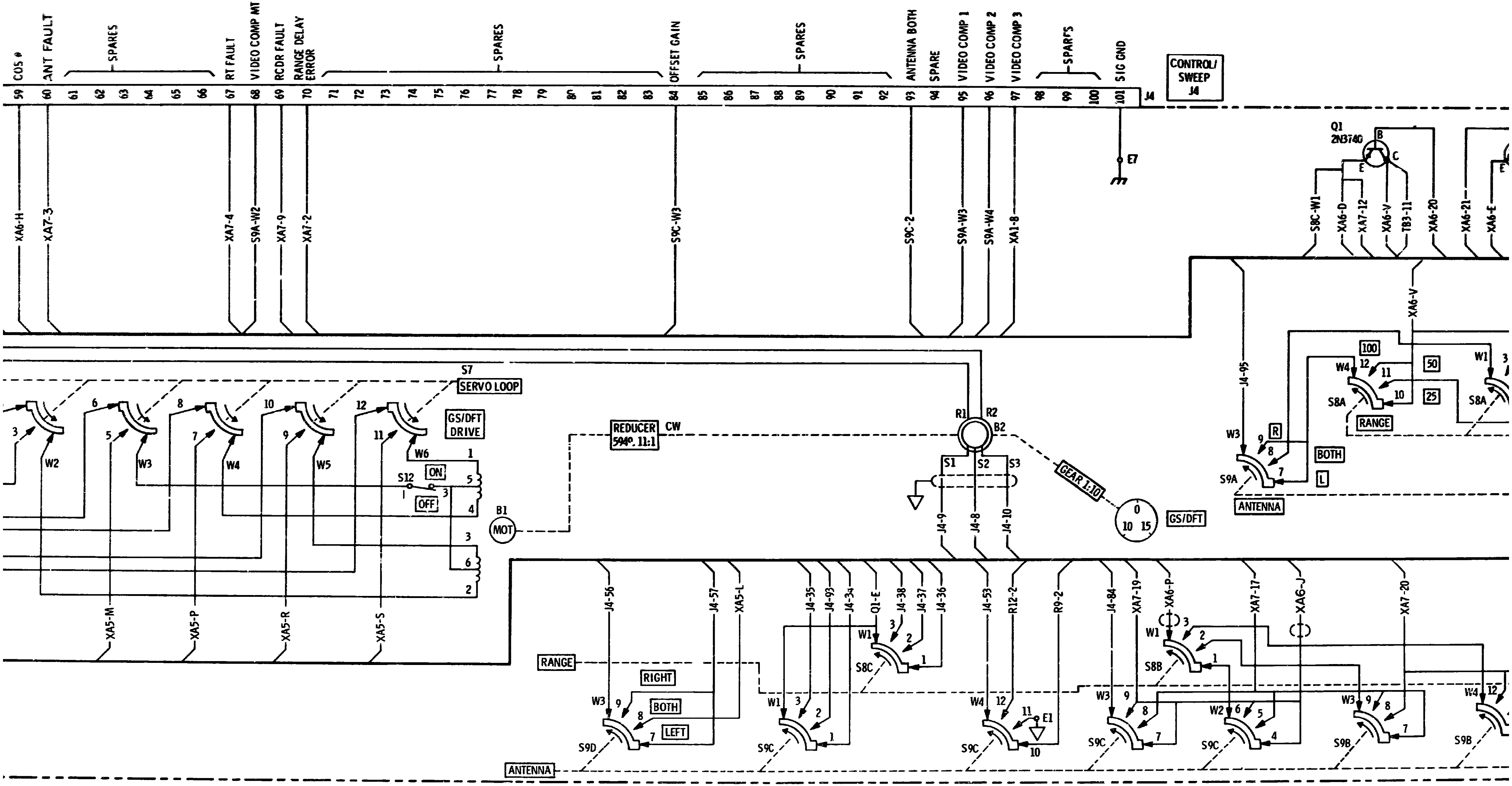


Figure FO-21. Test Set Subassembly MX-8639A/APS-94D, Unit 2 interconnection diagram (sheet 2 of 4)



DRIFT R2
DRIFT R1
SPARE
+28V CONT RTN
+28V CONT
+28V
+28V RTN
ANTENNA GATE
RGP FAULT
+15V
SECANT
-
+
CT
-15V
SPARES
ANTENNA LEFT
ANTENNA RIGHT
RANGE 25
RANGE 50
RANGE 100
SPARES
+20V
-20V
+20V RTN
SWEEP FAULT
IND FAULT
SPARE
VERT OFFSET
HORIZ OFFSET
FT BIAS
MT BIAS
VERT OFFSET VAR
VERT OFFSET VAR RTN
SIN θ
COS θ
ANT FAULT
SPARES
RT FAULT
VIDEO COMP MT
RCDR FAULT
RANGE DELAY ERROR
R22
4700
E7
XA5-14
XA5-11
S5-3
S5-2
XA5-K
XA1-10
XA7-5
XA6-V
XA6-X
S9C-1
S9C-3
S8C-1
S8C-2
S8C-3
E37
XA5-7
E44
XA6-C
XA5-15
XA7-7
XA7-8
R21-3
S9C-W4
XA1-X
XA1-Z
S9D-W3
S9D-7
XA6-R
XA6-H
XA7-3
XA7-4
S9A-W2
XA7-9
XA7-2
P
C
XA7-12
J4-23
DS4-2
S9D-8
XA6-C
J4-2
J4-1
XA7-6
E5
P/O XA5
A5 SERVO AMPLIFIERS
P/O XA5
J SERVO FAULT
5 26 VAC
13 26 VAC RTN
8 DRIFT
L -20V
K +28V RTN
10 GND SPEED
3
12 GND SPEED
11
14 DRIFT
9 NAV SIM ON
7
H +20V
15 20V RTN
GND SPEED MOTOR
DRIFT MOTOR
GND
SPARE
N
M
P
R
S
D
E
C
B
A
1
2
4
6
F
NAV
AUTO
S6
MANUAL
GS
J4-14
J4-15
J4-18
J4-17
J4-12
J4-46
XA6-B
J4-48
E5
E7
W1
W2
W3
W4
W5
S7-11
S7-9
S7-7
S7-5
E38
J1-61
XA5-M
XA5-P
XA5-R
D



CONTROL/ SWEEP J4
COS θ
ANT FAULT
SPARES
RT FAULT
VIDEO COMP MT
RCDR FAULT
RANGE DELAY ERROR
OFFSET GAIN
ANTENNA BOTH
SPARE
VIDEO COMP 1
VIDEO COMP 2
VIDEO COMP 3
SIG GND
Q1 2N3740
E7
S7
SERVO LOOP
GS/DFT DRIVE
ON
OFF
S12
B1
MOT
REDUCER 594°, 11:1
CW
R1 R2 B2
GEAR 1:10
GS/DFT
RANGE
RIGHT
BOTH
LEFT
ANTENNA
100
50
25
R
L
S8A
S9A
S8B
S8C
S9B
S9C
S9D
E1

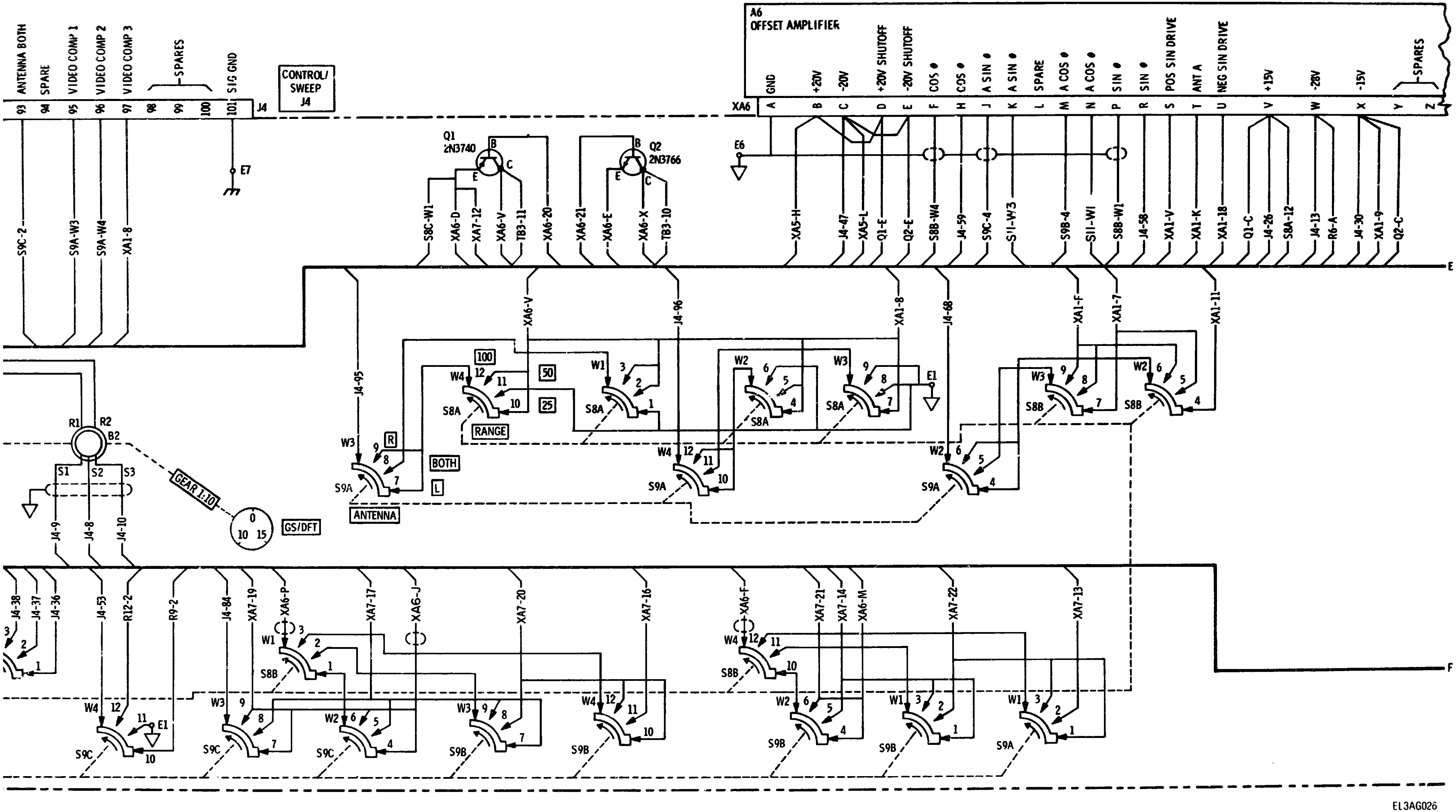


Figure FO-21. Test Set Subassembly MX-8639A/APS-94D, Unit 2 interconnection diagram (sheet 3 of 4)

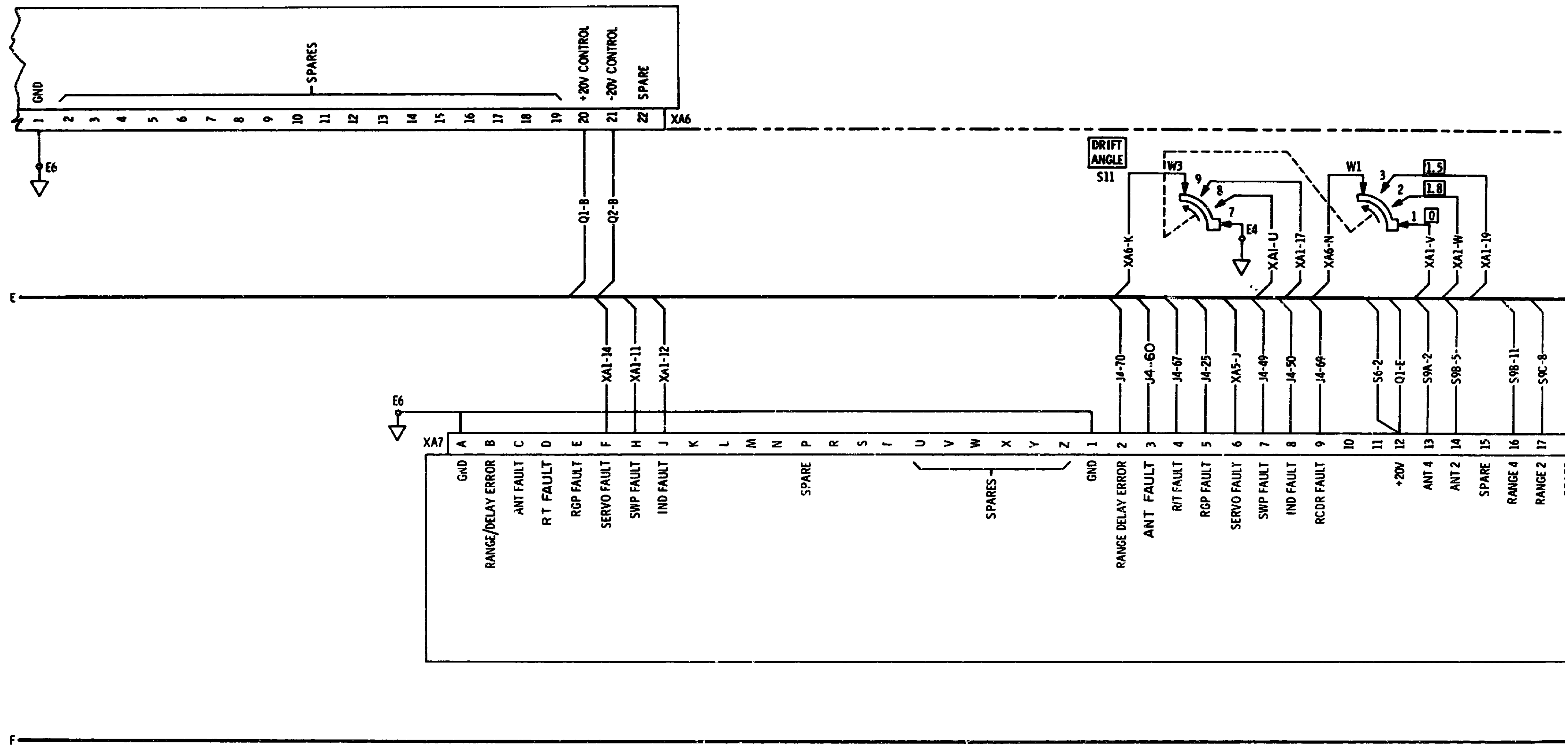


Figure FO-22. Yoke simulator, 2A1, schematic diagram

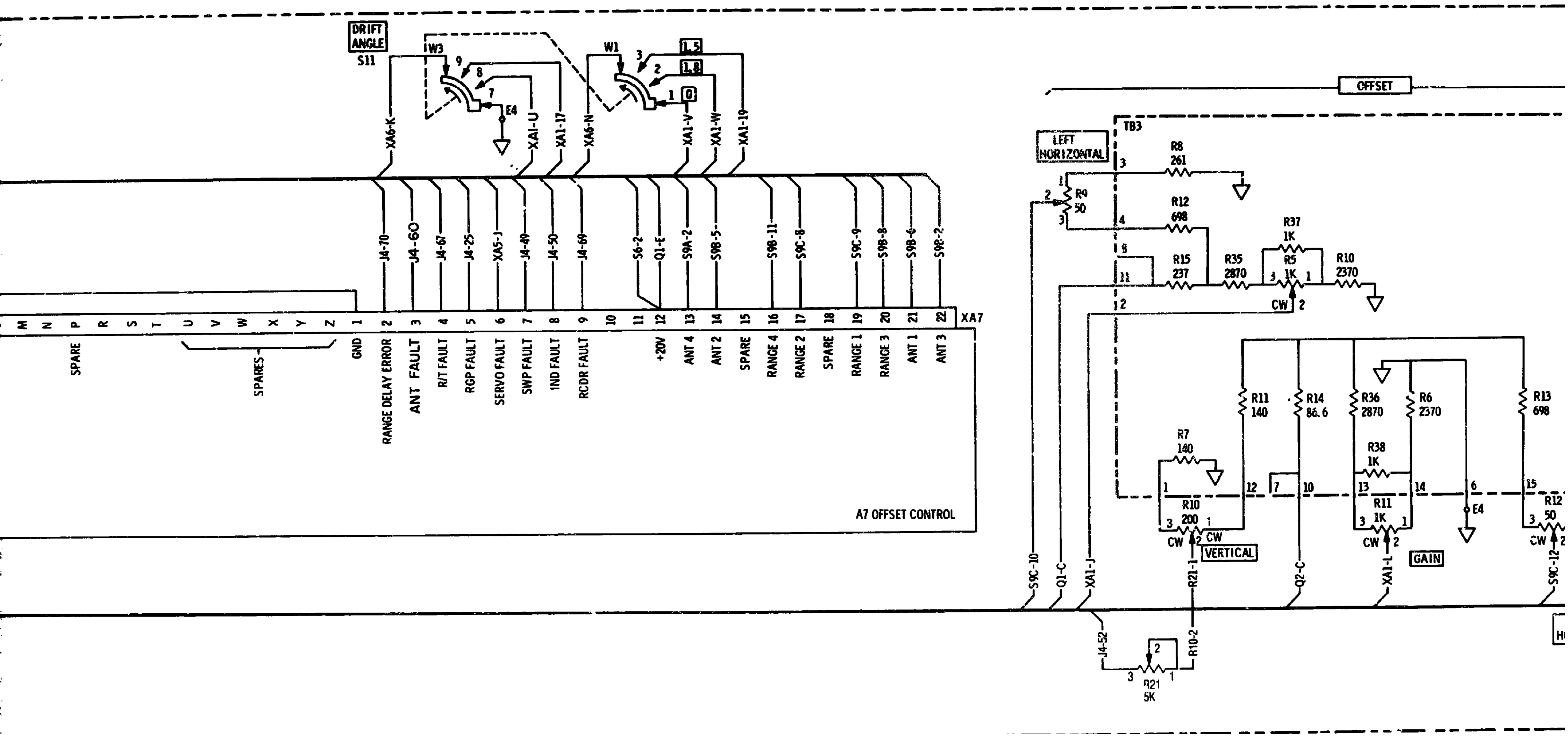
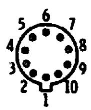


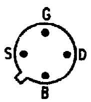
Figure FO-21. Test Set Subassembly MX-8639A/APS-94D, Unit 2 interconnection diagram

NOTES:

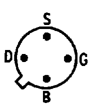
1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. FOR COMPLETE DESIGNATIONS PREFIX WITH 2A1.
2. UNLESS OTHERWISE SPECIFIED ALL RESISTORS ARE IN OHMS ALL CAPACITORS ARE IN μF.
3. INTEGRATED CIRCUIT DEVICE AR1 PIN ORIENTATION IS AS SHOWN BELOW.

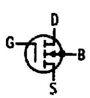


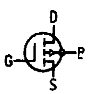
4. SEMICONDUCTOR DEVICE Q12 AND Q13 PIN ORIENTATION IS AS SHOWN BELOW.



5. SEMICONDUCTOR DEVICE Q2 PIN ORIENTATION IS AS SHOWN BELOW.



6.  INDICATES N CHANNEL MOS-16FET DESIGNED FOR ENHANCEMENT-MODE OPERATION

7.  INDICATES P CHANNEL MOS-16FET DESIGNED FOR ENHANCEMENT-MODE OPERATION.

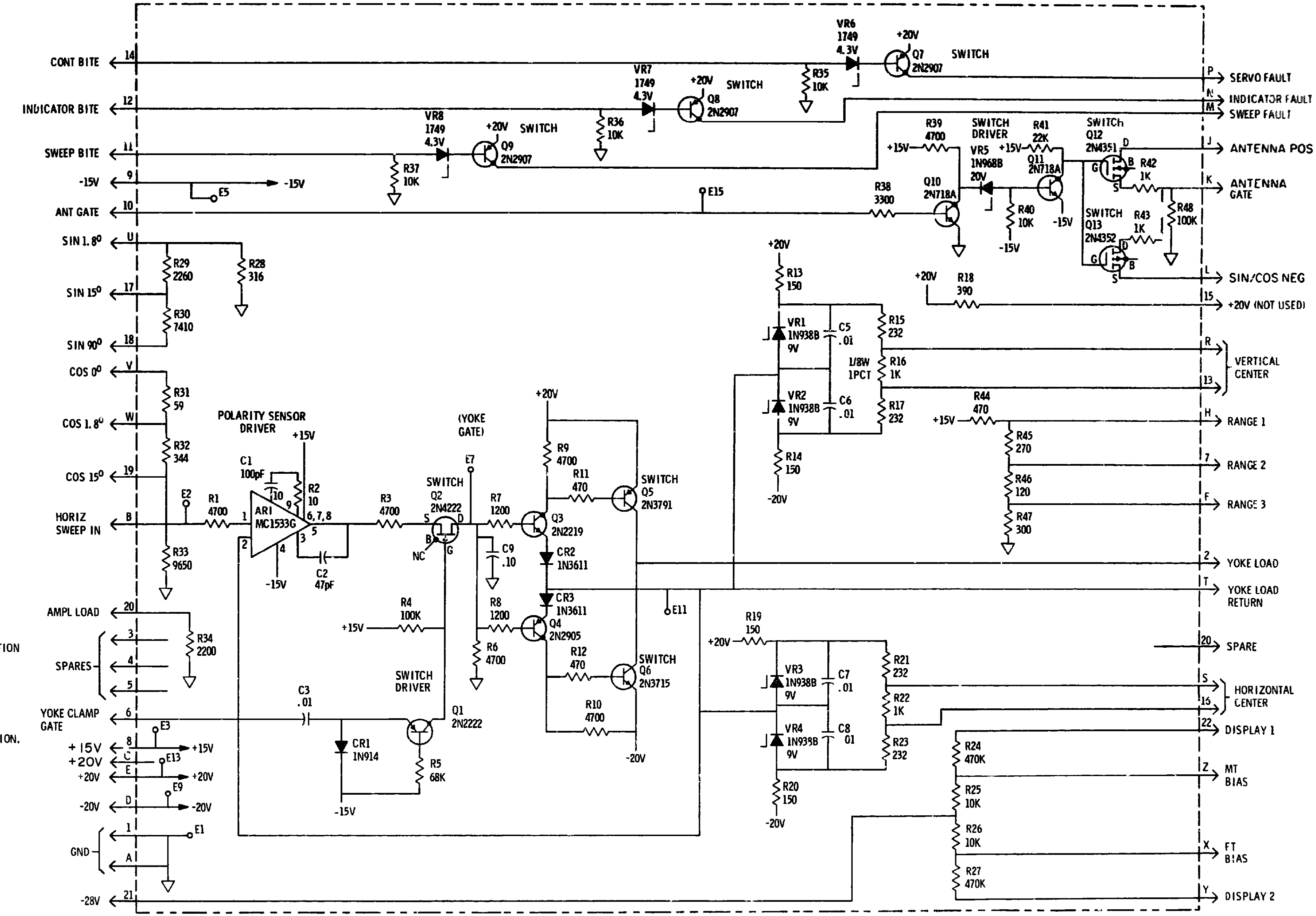


Figure FO-22. Yoke simulator, 2A1, schematic diagram

NOTES:

1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. FOR COMPLETE DESIGNATIONS PREFIX WITH 2A2, 2A3.
2. UNLESS OTHERWISE SPECIFIED:
   ALL RESISTORS ARE IN OHMS
   ALL CAPACITORS ARE IN µF.
3. CONNECTOR VIEWED FROM MATING SIDE.
4. PIN ORIENTATION OF Q1 IS SHOWN BELOW:

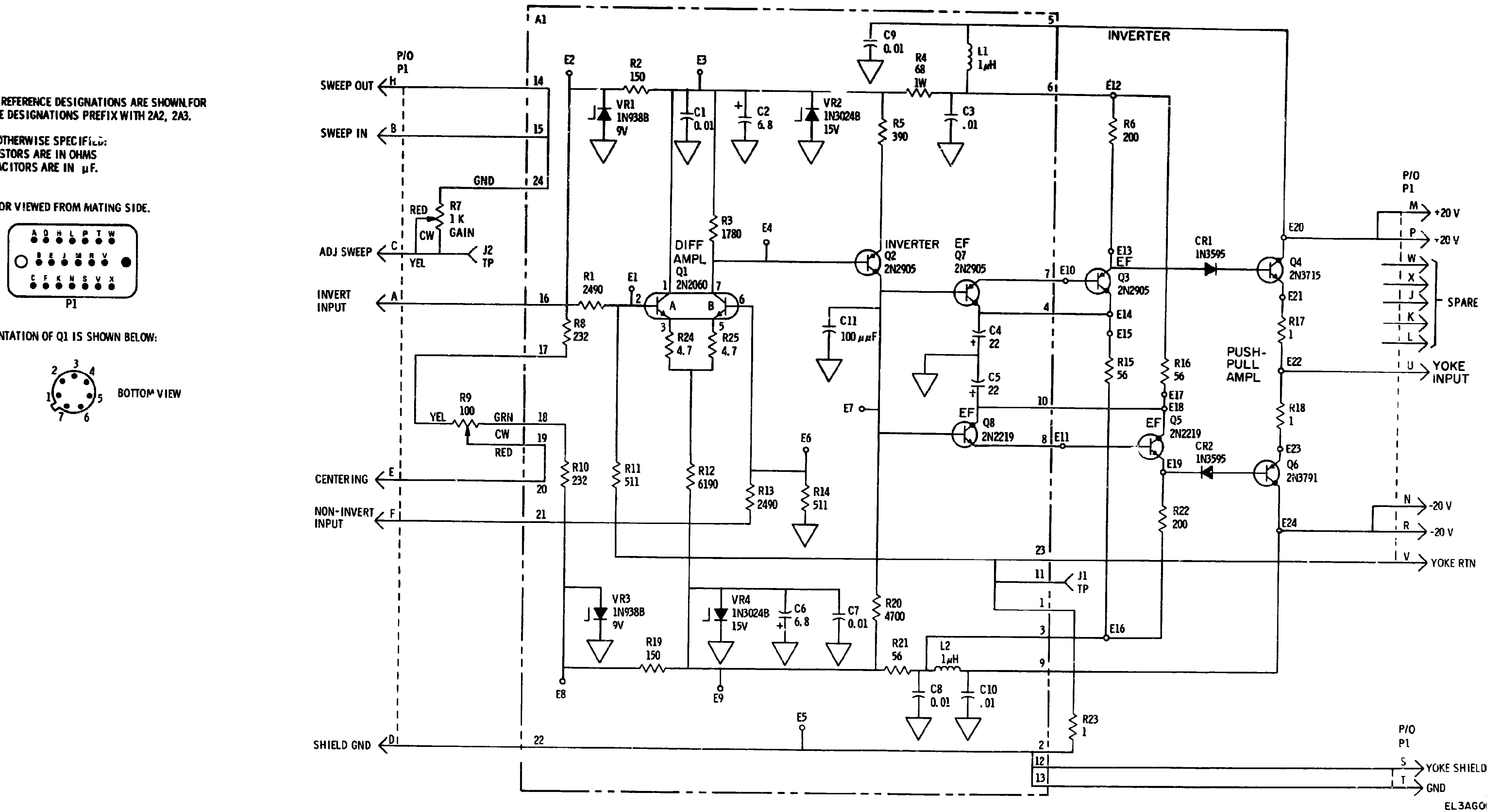


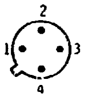
Figure FO-23. Direct current amplifiers, 2A2/2A3, schematic diagram

NOTES

1 PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. FOR COMPLETE DESIGNATIONS PREFIX WITH 2A4.

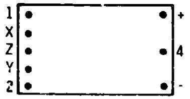
2. UNLESS OTHERWISE SPECIFIED ALL RESISTORS ARE IN OHMS ALL CAPACITORS ARE IN pF

3. SEMICONDUCTOR DEVICES A1Q3 4, 5, 6, 7, 8, 9, 10, AND A2Q1 & 2 PIN ORIENTATION IS AS SHOWN BELOW



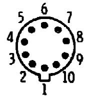
BOTTOM VIEW

4 INTEGRATED CIRCUIT DEVICES A1AR1, 2 5, 6, 7 8, AND A2AR2, 4, 5, 6, 7 8, 9, 10 11 12 & 13 PIN ORIENTATION IS AS SHOWN BELOW



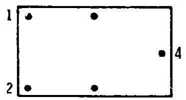
BOTTOM VIEW

5 INTEGRATED CIRCUIT DEVICES A1AR3 AND A2AR1 & 3 PIN ORIENTATION IS AS SHOWN BELOW



BOTTOM VIEW

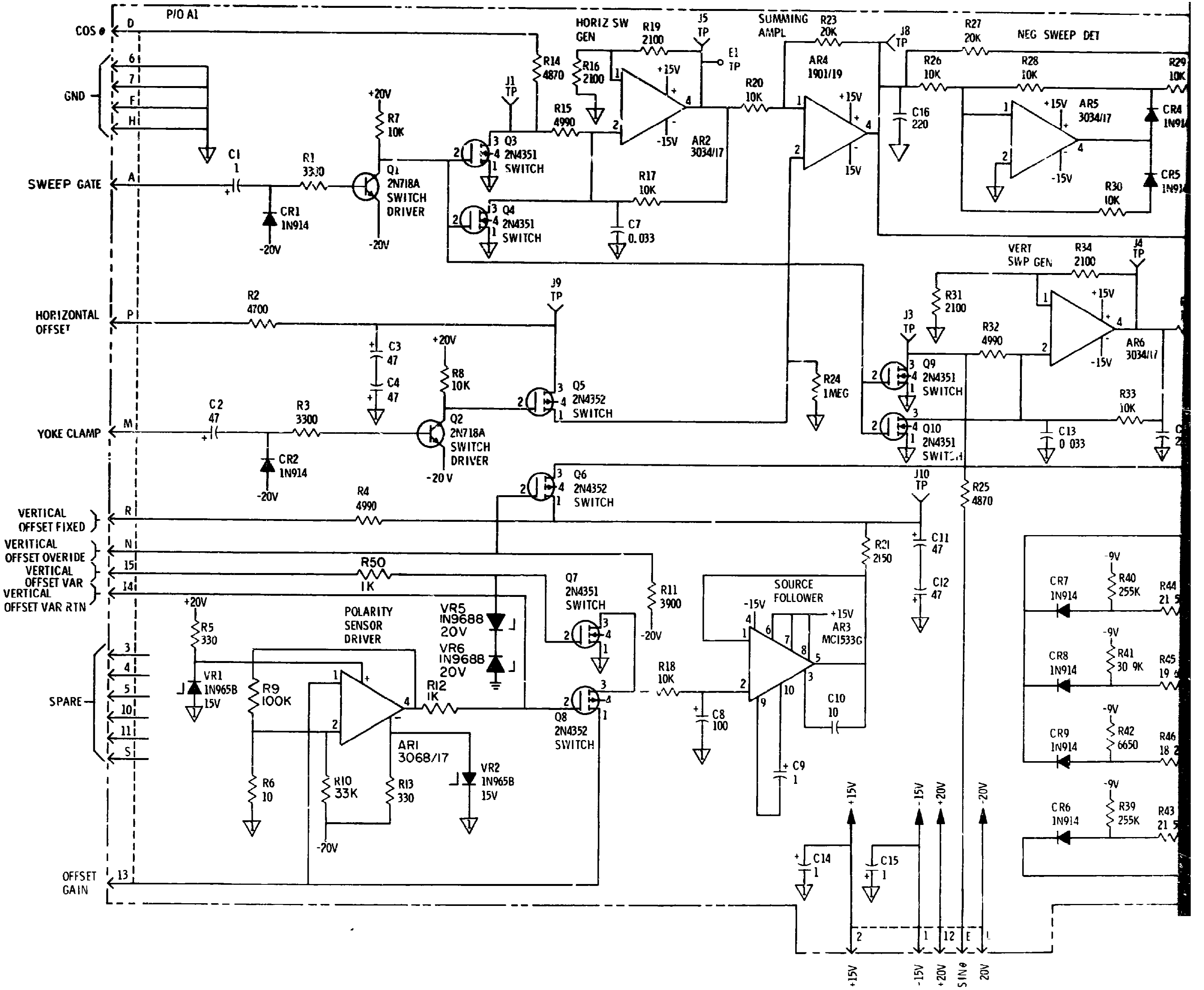
6. INTEGRATED CIRCUIT DEVICE A1AR4 & 9 PIN ORIENTATION IS AS SHOWN BELOW



BOTTOM VIEW

7  SYMBOL MEANS N-CHANNEL INSULATED GATE ENHANCEMENT TYPE SINGLE GATE MOS-FET.

8  SYMBOL MEANS P-CHANNEL INSULATED GATE ENHANCEMENT TYPE SINGLE GATE MOS-FET.



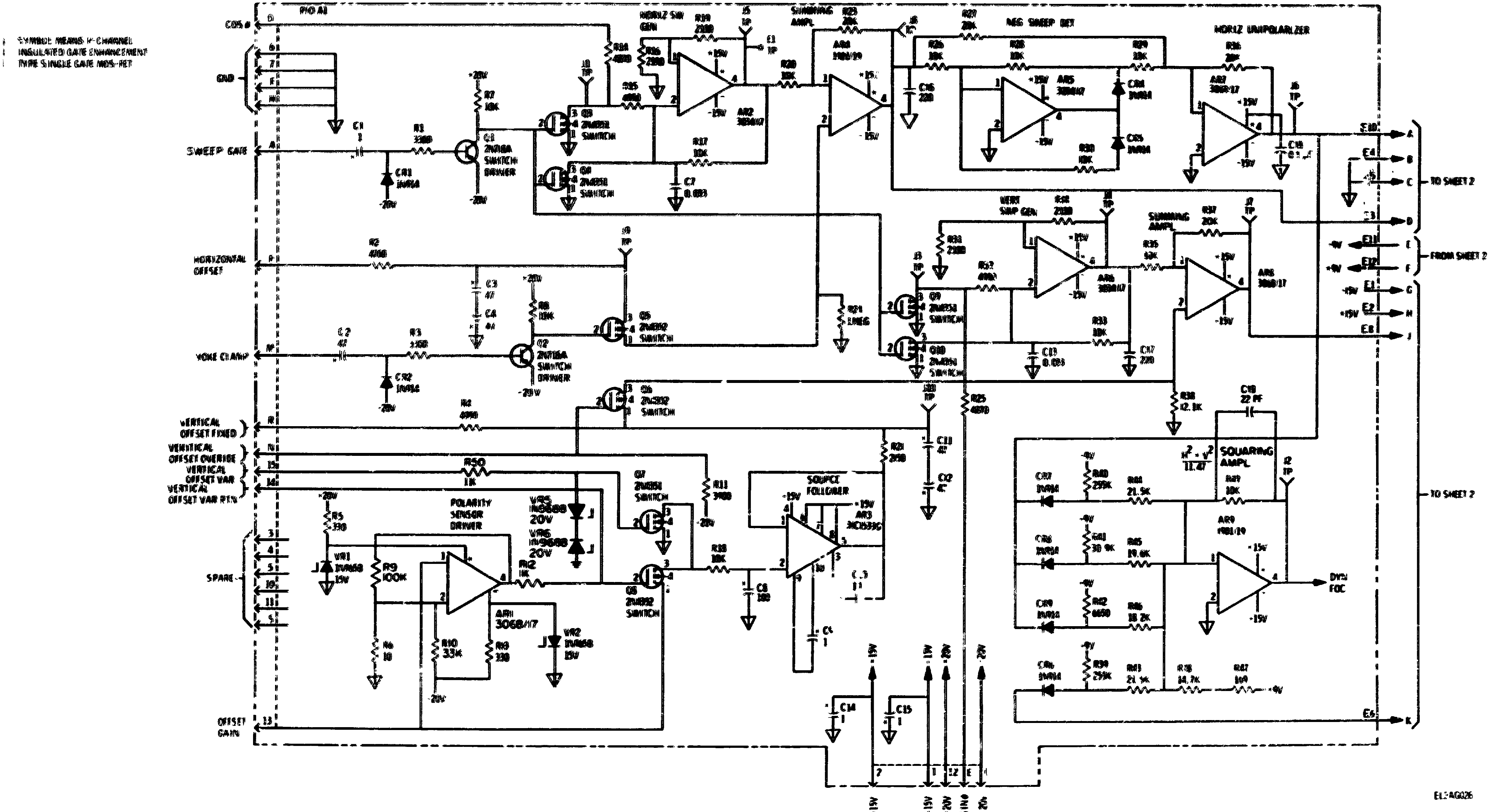


Figure FO-24. Sweep generator, 2A4, schematic diagram (sheet 1 of 2)

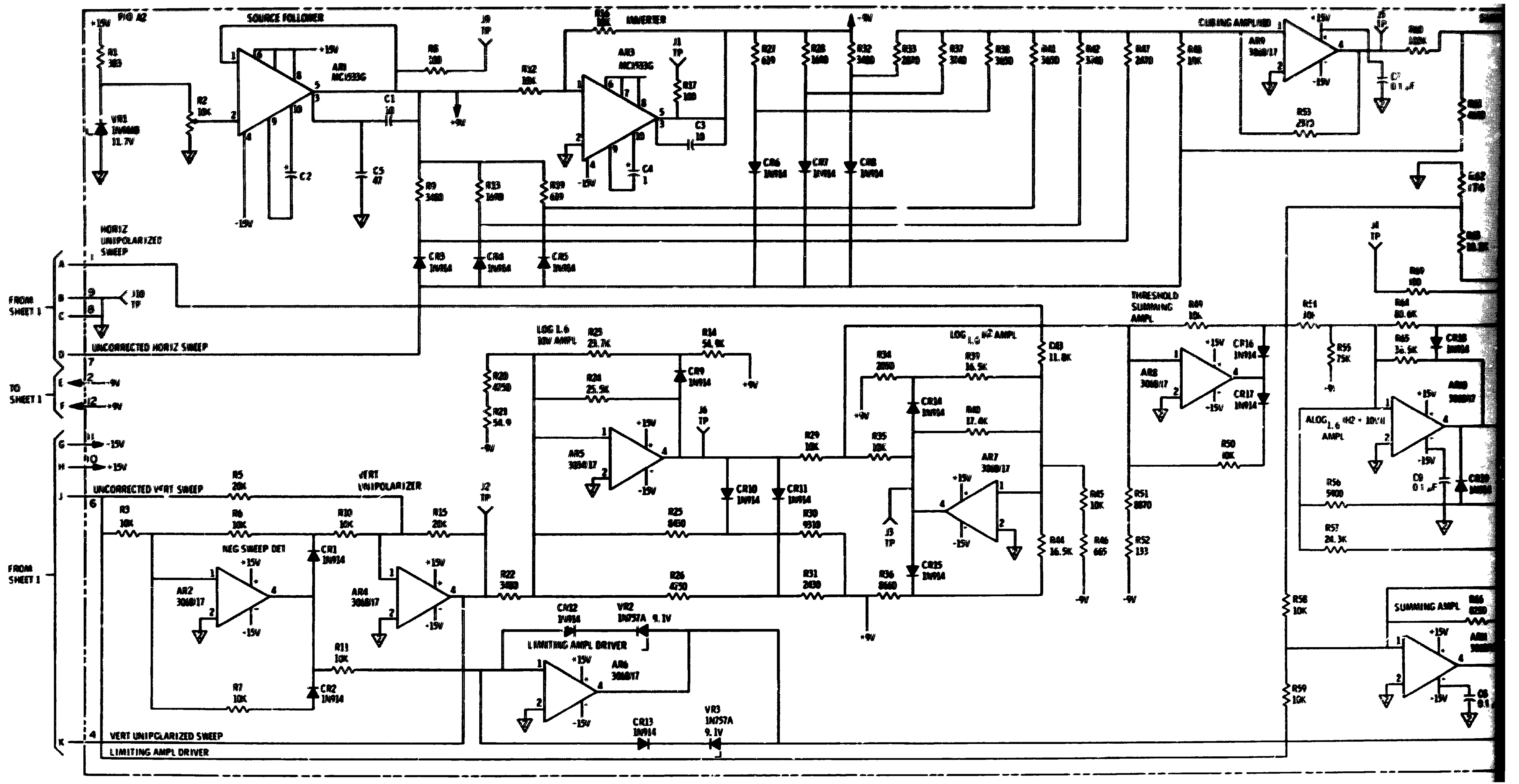


FIG A2
SOURCE FOLLOWER
INVERTER
CUBING AMPLIFIER
HORIZ UNIPOLARIZED SWEEP
FROM SHEET 1
UNCORRECTED HORIZ SWEEP
TO SHEET 1
UNCORRECTED VERT SWEEP
VERT UNIPOLARIZER
NEG SWEEP DET
LOG 1.6 10V AMPL
LOG 1.6 AMPL
THRESHOLD SUMMING AMPL
LIMITING AMPL DRIVER
SUMMING AMPL
VERT UNIPOLARIZED SWEEP
LIMITING AMPL DRIVER

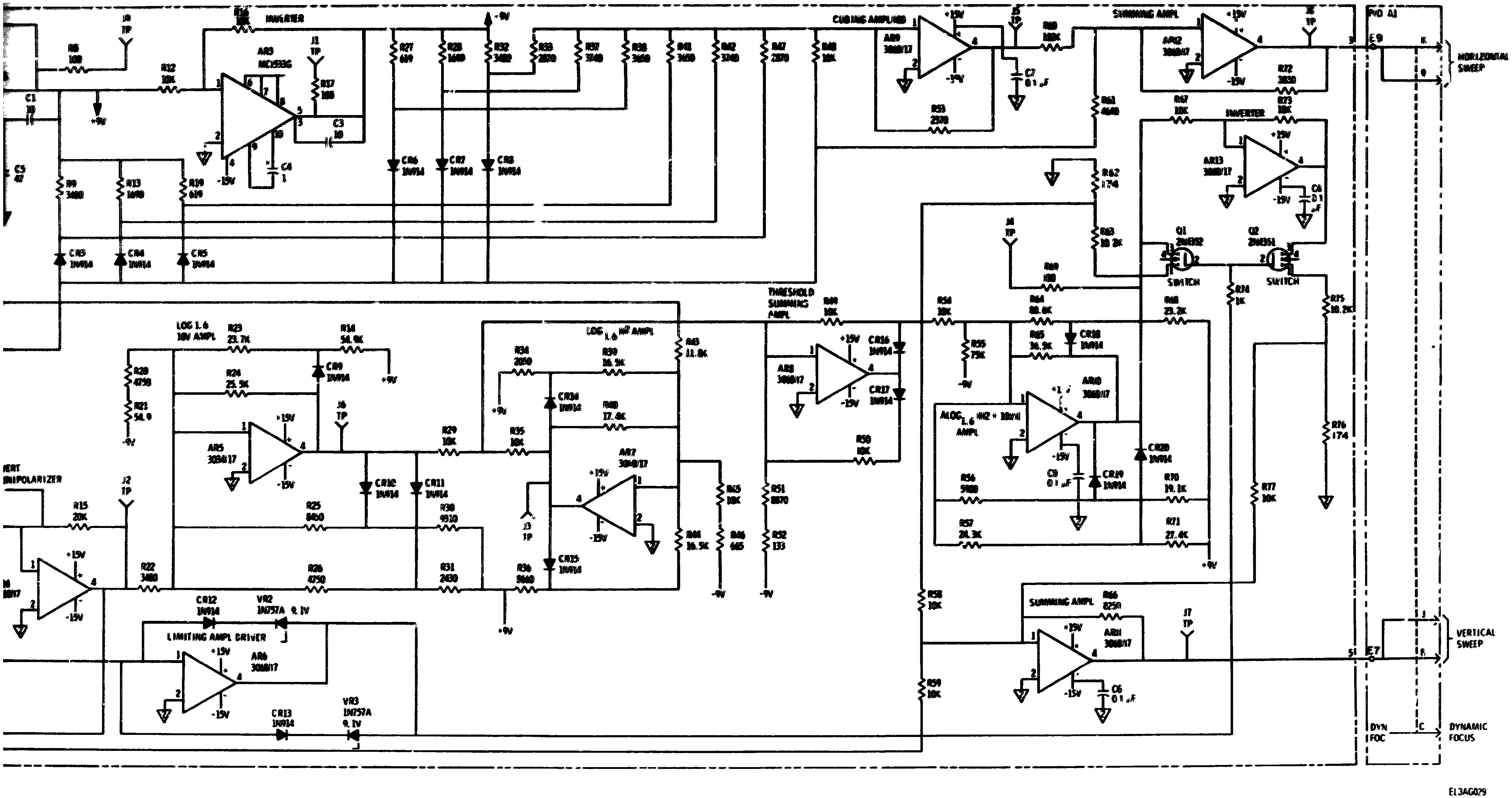


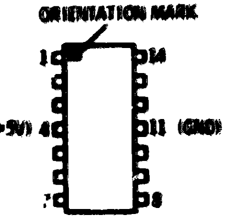
Figure FO-24. Sweep generator, 2A4, schematic diagram (sheet 2 of 2)

NOTES:

1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. FOR COMPLETE DESIGNATIONS PREFIX WITH 2A5.

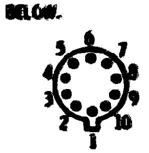
2. UNLESS OTHERWISE SPECIFIED ALL RESISTORS ARE IN OHMS ALL CAPACITORS ARE IN μF ALL INDUCTORS ARE IN μH

3. INTEGRATED CIRCUIT DEVICES U1 THRU U12 HAVE PARTIAL TYPE NUMBERS SHOWN. FOR COMPLETE TYPE NUMBER PREFIX WITH S8 AND SUFFIX WITH J. EXAMPLE: 880 - SHOWN S8880J - TYPE NO. PIN ORIENTATION IS AS SHOWN BELOW.



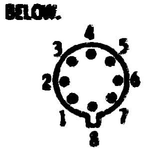
TOP VIEW

4. INTEGRATED CIRCUIT DEVICES A3AR1, 2, 5, AND 6 PIN ORIENTATION IS AS SHOWN BELOW.



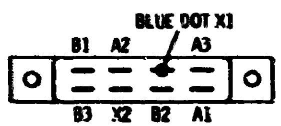
BOTTOM VIEW

5. INTEGRATED CIRCUIT DEVICES A3AR3, 4, 7, AND 8 PIN ORIENTATION IS AS SHOWN BELOW.

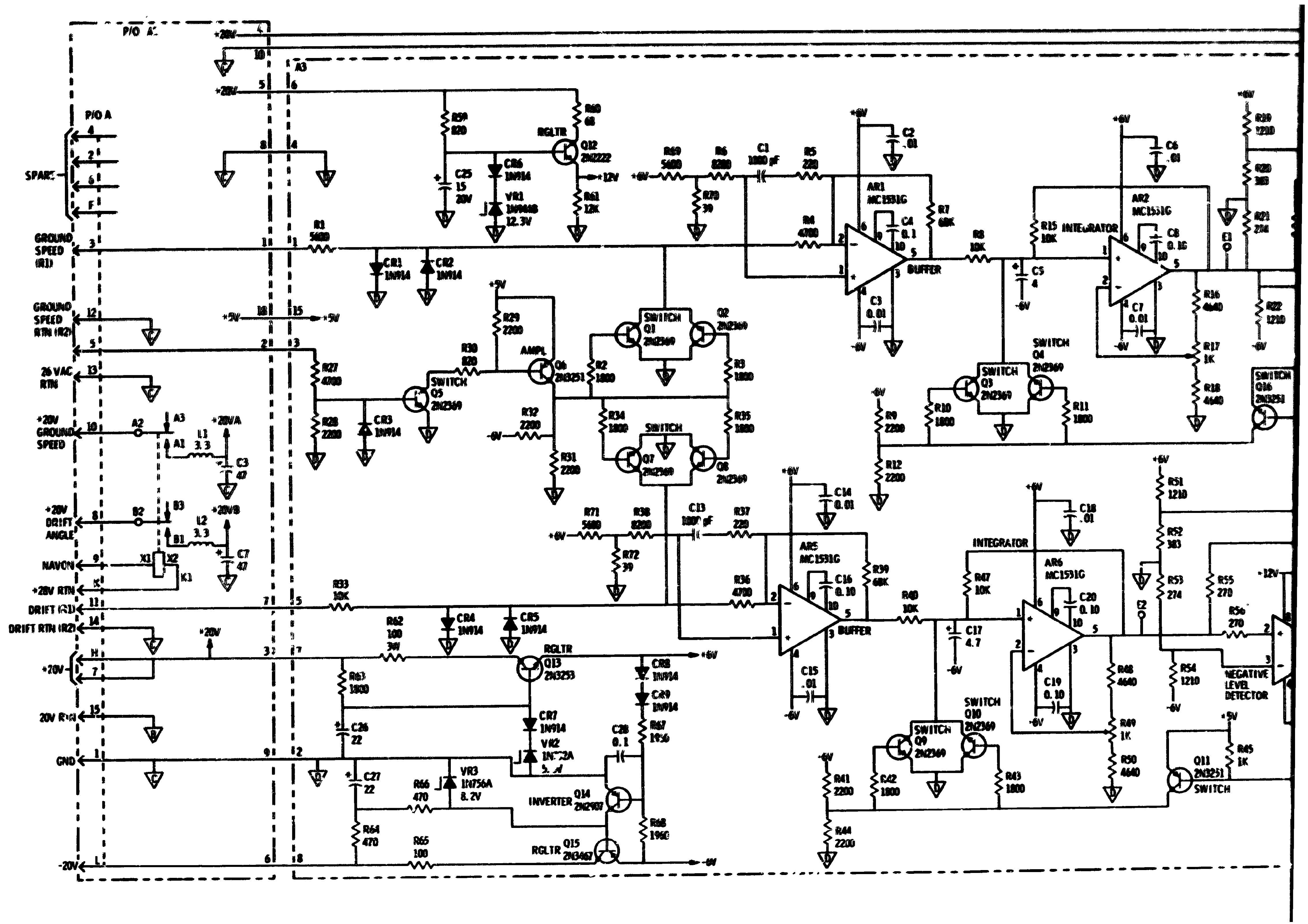


BOTTOM VIEW

6. RELAY A2K1 IS SHOWN IN DE-ENERGIZED STATE. PIN ORIENTATION IS AS SHOWN BELOW.



BOTTOM VIEW



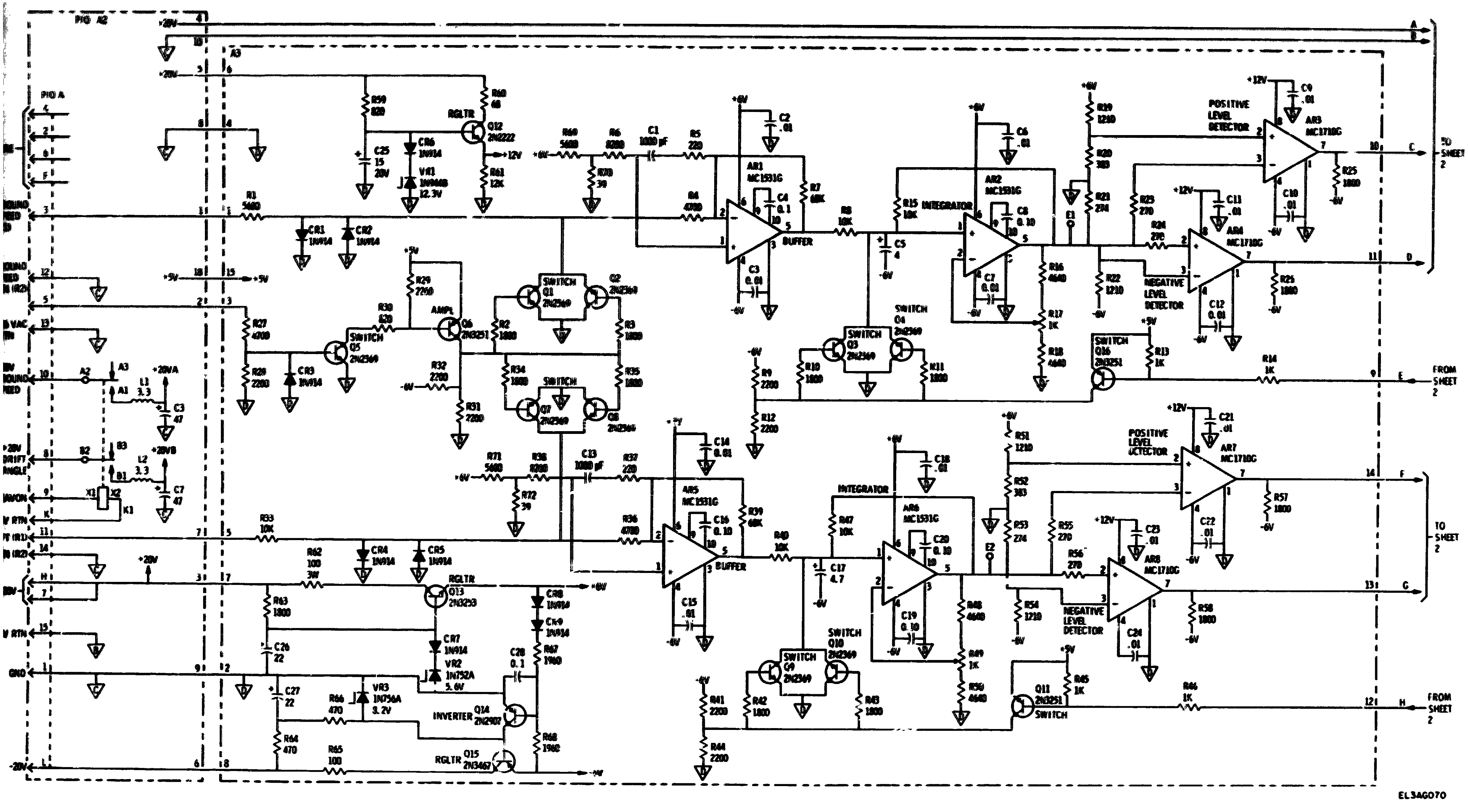
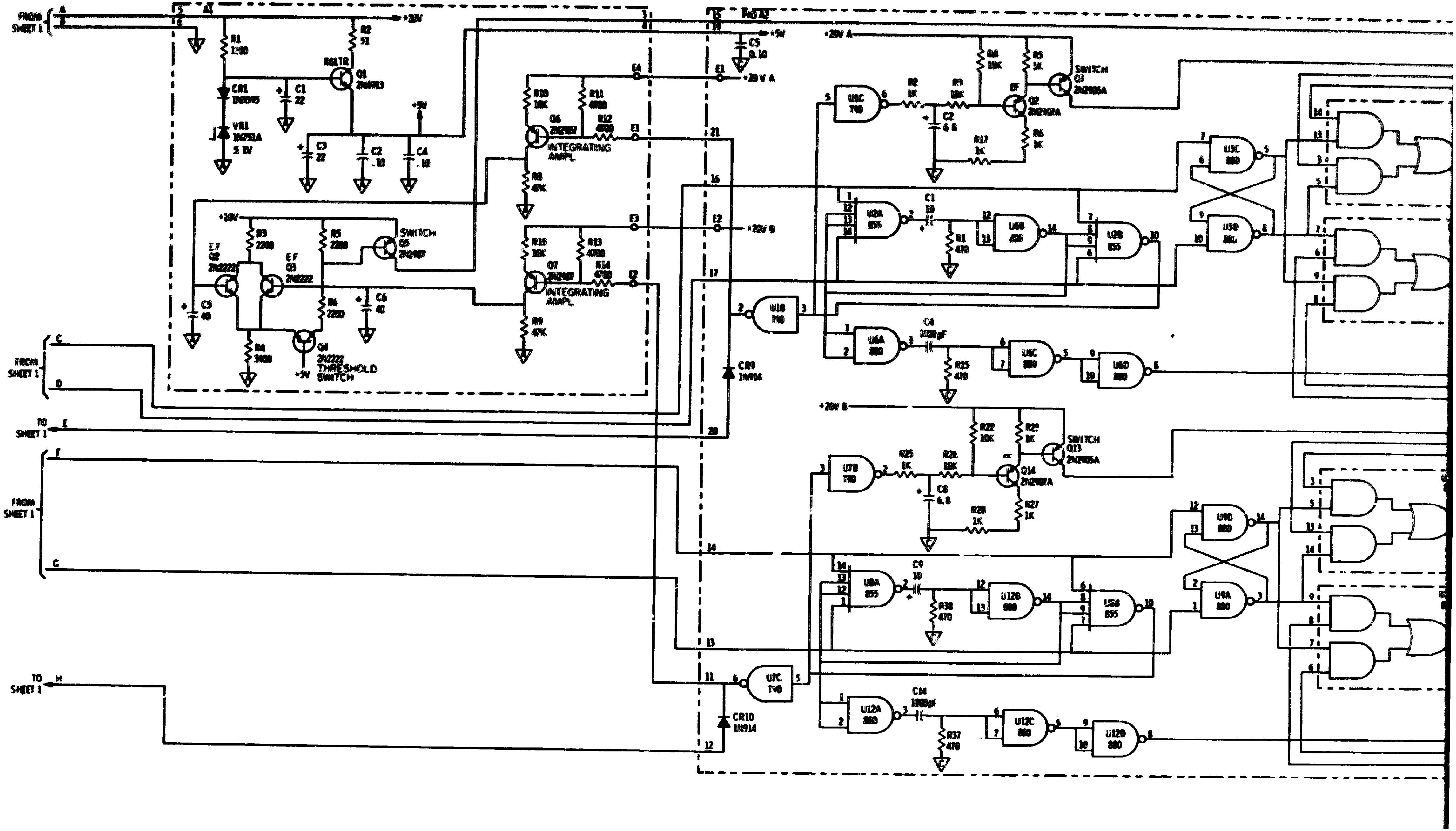


Figure FO-25,. servoamplifer, 2A5, schematic diagram (sheet 1 of 2).


FROM SHEET 1
A1
+20V
R1 1200
R2 51
RGLTR Q1
CR1
VR1 5.1V
C1 22
C3 22
C2 .10
C4 .10
+5V
E4
E1
+20 V A
R10 10K
R11 4700
R12 4700
Q6
INTEGRATING AMPL
R8 47K
SWITCH Q5
R3 2200
R5 2200
EF Q2 2N2222
EF Q3 2N2222
C5 40
R6 2200
C6 40
R4 3900
Q4 2N2222
THRESHOLD SWITCH
E3
E2
+20V B
R15 10K
R13 4700
R14 4700
Q7
INTEGRATING AMPL
R9 47K
FROM SHEET 1
TO SHEET 1
FROM SHEET 1
TO SHEET 1
A2
C5 0.10
+20V A
R4 10K
R5 1K
SWITCH Q1 2N2905A
U1C T90
R2 1K
R3 10K
C2 6.8
Q2 2N2907A
R6 1K
R17 1K
U3C 880
U3D 880
U2A 855
C1 10
R1 470
U2B 855
U1B T90
CR9 1N914
U6A 880
C4 1000 pF
U6C 880
U6D 880
R35 470
+20V B
R22 10K
R21 1K
SWITCH Q13 2N2905A
U7B T90
R25 1K
R26 10K
Q14 2N2907A
C8 6.8
R28 1K
R27 1K
U9D 880
U8A 855
C9 10
R38 470
U12B 880
U8B 855
U9A 880
U7C T90
CR10 1N914
U12A 880
C14 1000pF
U12C 880
U12D 880
R37 470

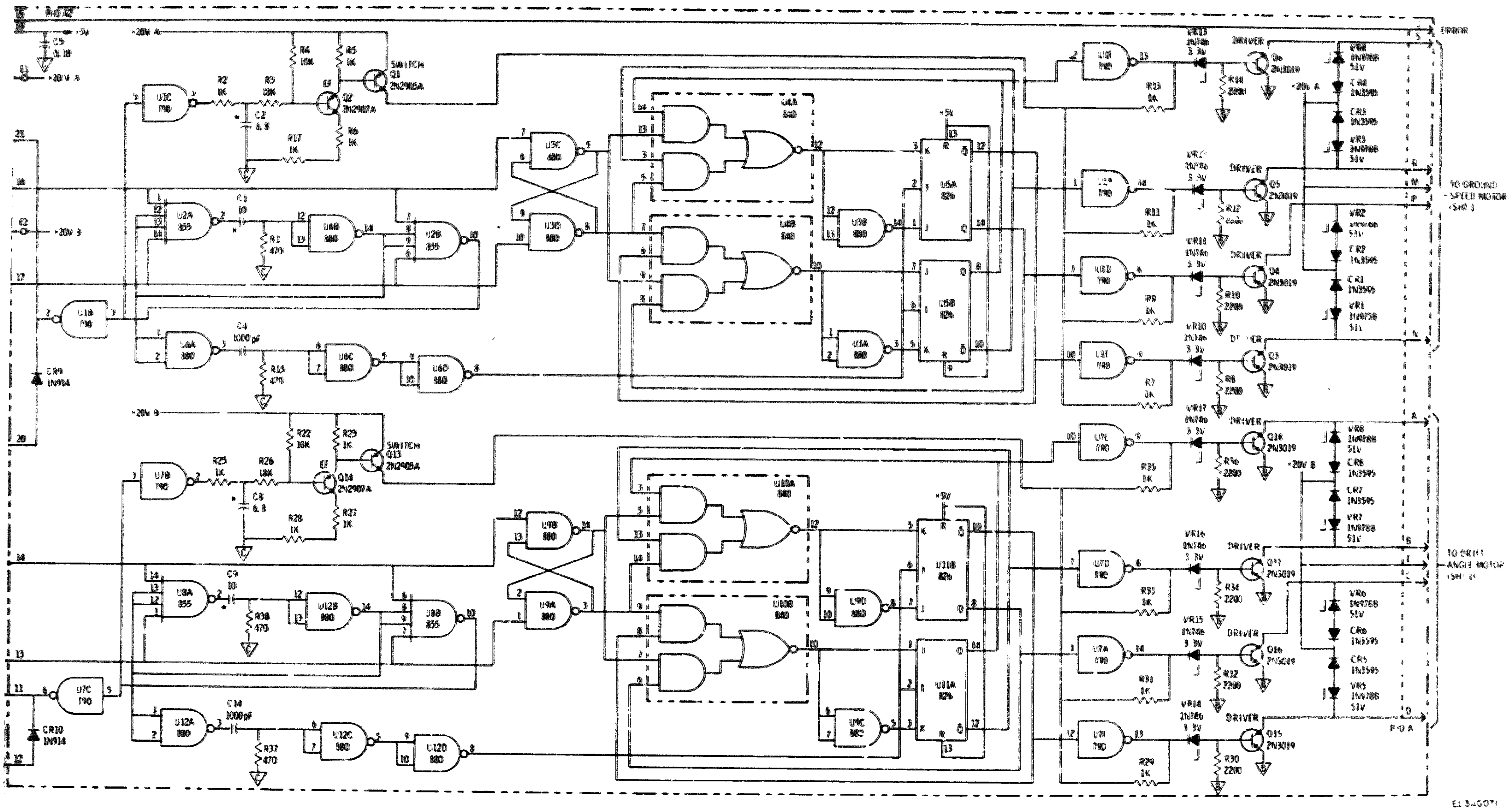


Figure FO-25. Servoamplifer, 2A5 schematic diagram (sheet 2 of 2)

NOTES

1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN FOR COMPLETE DESIGNATIONS PREFIX WITH 2A6.
2. UNLESS OTHERWISE SPECIFIED ALL RESISTORS ARE IN OHMS. ALL CAPACITORS ARE IN µF.
3. INTEGRATED CIRCUIT DEVICES 2A6A1AR1, 2,3,4,5, AND 6 PIN ORIENTATION IS AS SHOWN BELOW
4. SEMICONDUCTOR DEVICES A1Q2 AND A1Q4 PIN OR ORIENTATION IS AS SHOWN BELOW
5. INTEGRATED CIRCUIT DEVICES 2A6A1AR1, 3, 4, 5 AND 6. PIN 4 CONNECTS TO -15V AND PINS 6, 7, & 8 CONNECT TO +15V

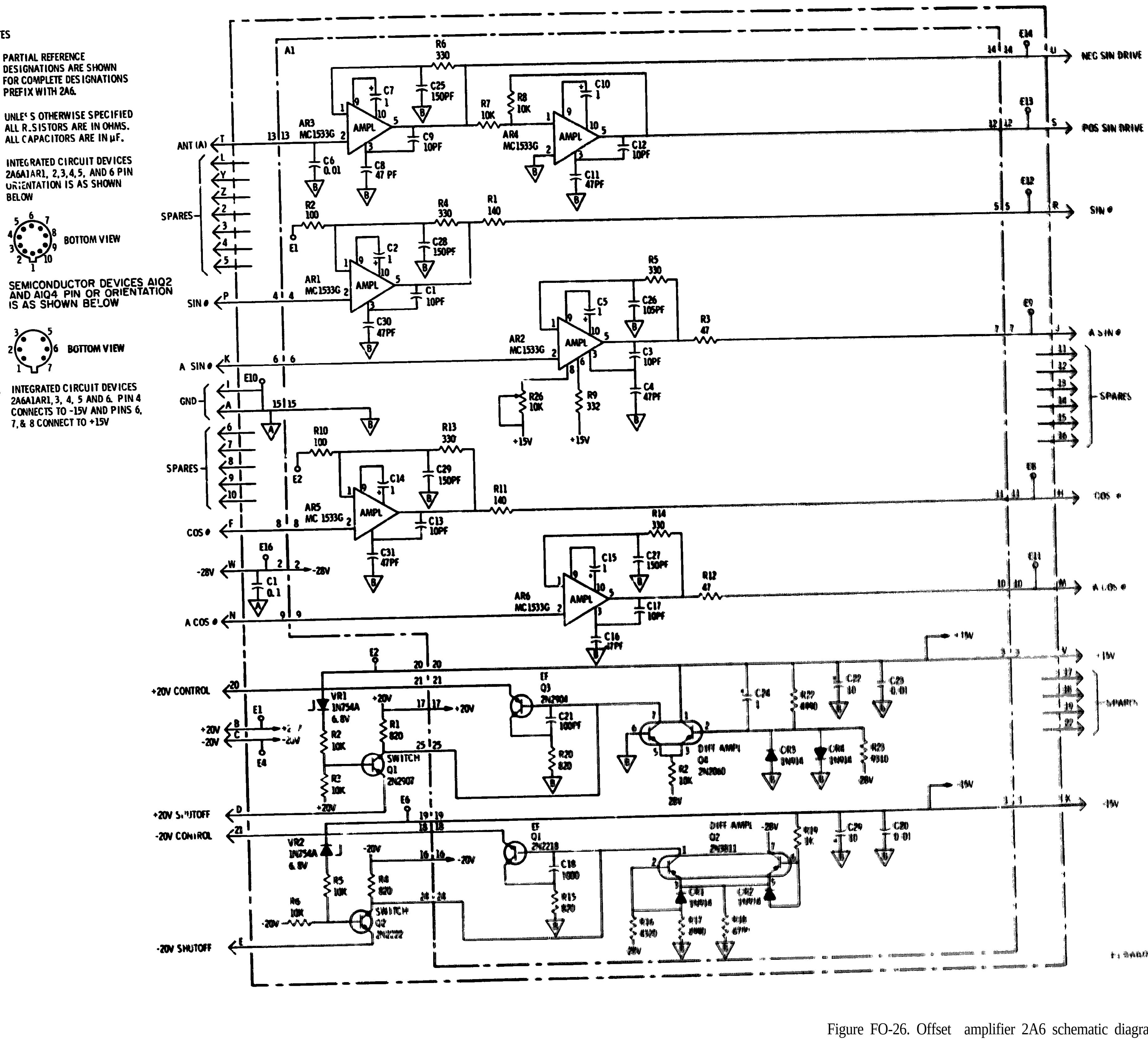
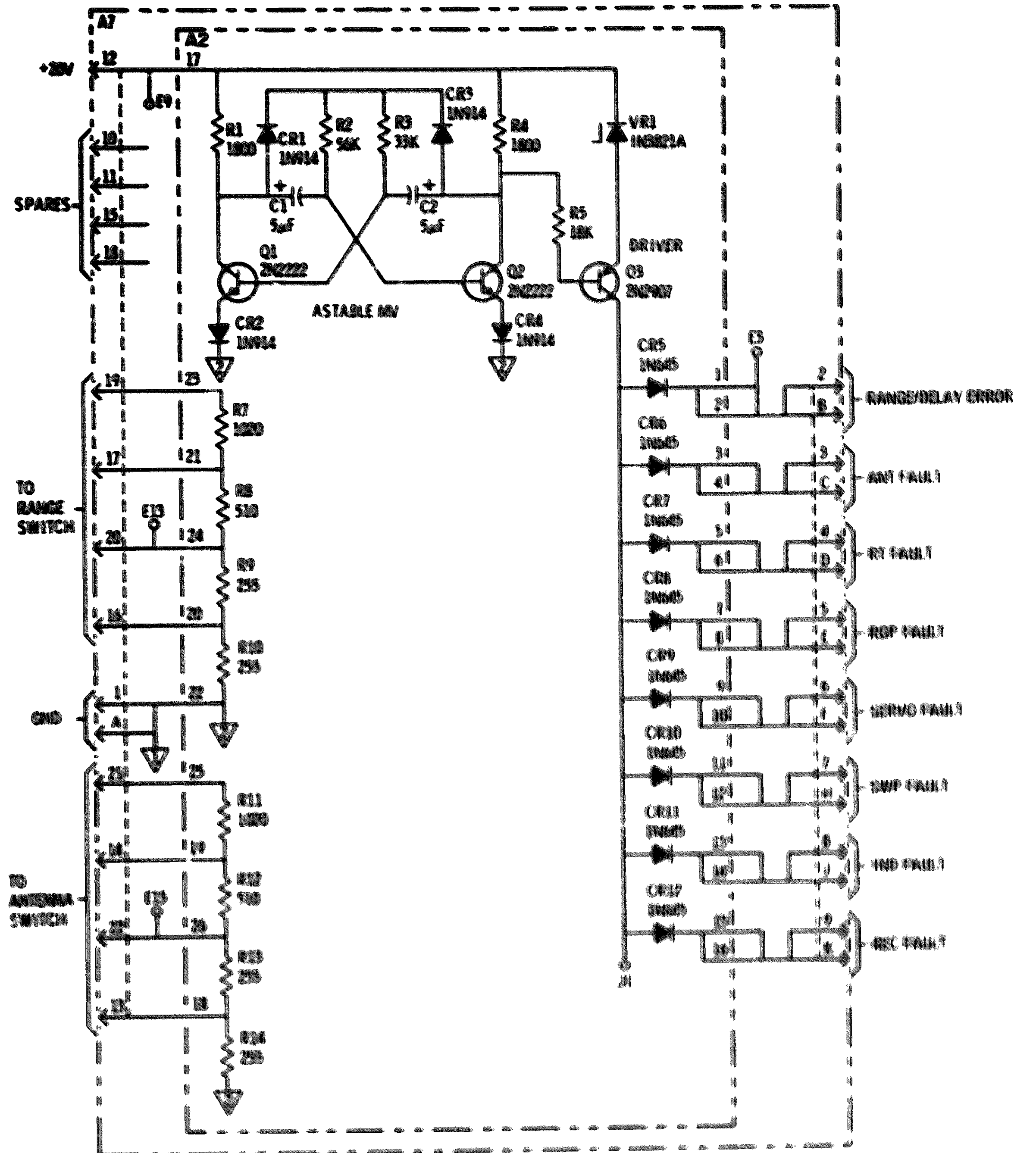


Figure FO-26. Offset amplifier 2A6 schematic diagram



NOTES

Figure FO-27. [illegible]

Order of the Secretary of the Army:

BERNARD W. ROGERS
General, United States Army
Chief of Staff

icial:

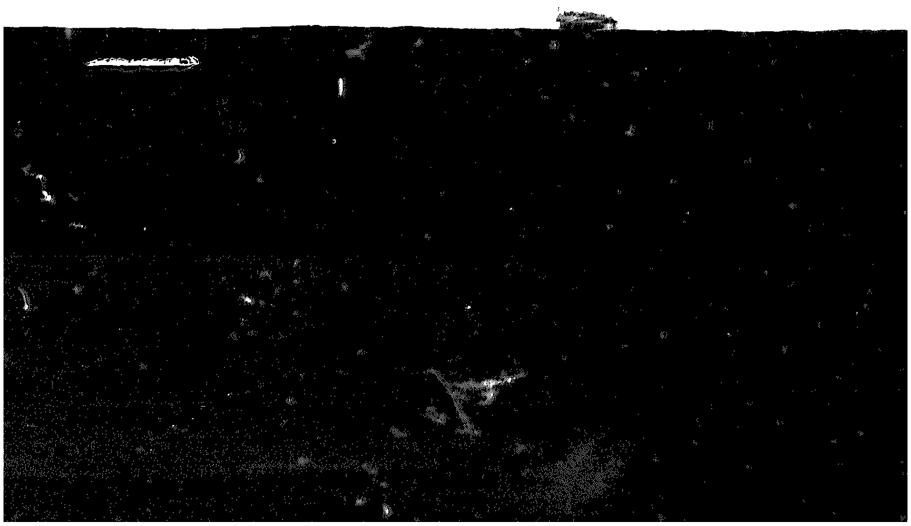
J. C. PENNINGTON
ior General, United States Army
The Adjutant General

TRIBUTION:
To be distributed in accordance with DA Form 12–36, Direct and General Support maintenance require-
its for AN/APS–94.

END

03-17-83

DATE



DEPARTMENT OF THE ARMY

MICROFORM TEST TARGET

150 MM

1.0 mm (e= .81 mm)

ABCDEFGHIJKLMNOPQRSTUVWXYZ1234567890
abcdefghijklmnopqrstuvwxyz$¢£/%#½¼¾—=+×&@*

1.5 mm (e= 1.09 mm)

ABCDEFGHIJKLMNOPQRSTUVWXYZ1234567890
abcdefghijklmnopqrstuvwxyz$¢£/%#½¼¾—=+×&@*

2.0 mm (e= 1.37 mm)

ABCDEFGHIJKLMNOPQRSTUVWXYZ
abcdefghijklmnopqrstuvwxyz
1234567890$¢£/%#½¼¾—=+×&@*

2.5 mm (e= 1.77 mm)

ABCDEFGHIJKLMNOPQRSTUVWXYZ
abcdefghijklmnopqrstuvwxyz
1234567890$¢£/%#½¼¾—=+×&@*

1.0 mm (e= .81 mm)

ABCDEFGHIJKLMNOPQRSTUVWXYZ1234567890
abcdefghijklmnopqrstuvwxyz$¢£/%#½¼¾—=+×&@*

1.5 mm (e= 1.09 mm)

ABCDEFGHIJKLMNOPQRSTUVWXYZ1234567890
abcdefghijklmnopqrstuvwxyz$¢£/%#½¼¾—=+×&@*

2.0 mm (e= 1.37 mm)

ABCDEFGHIJKLMNOPQRSTUVWXYZ
abcdefghijklmnopqrstuvwxyz
1234567890$¢£/%#½¼¾—=+×&@*

2.5 mm (e= 1.77 mm)

ABCDEFGHIJKLMNOPQRSTUVWXYZ
abcdefghijklmnopqrstuvwxyz
1234567890$¢£/%#½¼¾—=+×&@*

200 MM

250 MM